2026 IEEE International Conference on Integrated Circuits, Technologies & Applications

ICTA 2026

ADVANCING IC WITH AI

21 - 24 October 2026
Grand Corpthorne Waterfront Hotel, Singapore

CONFERENCE PROGRAM BOOKLET



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CONFERENCE VENUE

Grand Copthorne Waterfront Hotel Singapore

Address: 392 Havelock Road Singapore 169663



Transportation to Conference Venue

MRT Route:

Travel Time: **~50 minutes**
(Note: Requires 8–10 minutes of walking or a short bus/taxi ride at the end)

1. At Changi Airport MRT Station (CG2), board the Green Line (East-West Line) toward Tanah Merah (EW4).
2. At Tanah Merah, transfer to the train going toward Tuas Link.
3. Alight at Outram Park MRT Station.
4. Transfer to the Thomson-East Coast Line (TEL) toward Woodlands.
5. Alight at Havelock MRT Station (TE16) — this is the closest station to the hotel.
6. From Havelock MRT Station, take Exit 4 and walk ~10 minutes to the hotel.

Public Bus Route:

Travel Time: **~50-60 minutes**

1. From the airport, take Bus 36/36B.
2. Alight at Aft Havelock Rd bus stop (Stop ID: 06169)
3. Walk 3–5 minutes to Grand Copthorne Waterfront Hotel.

Ride Booking App are widely used in Singapore. (Grab, Gojek, TADA):

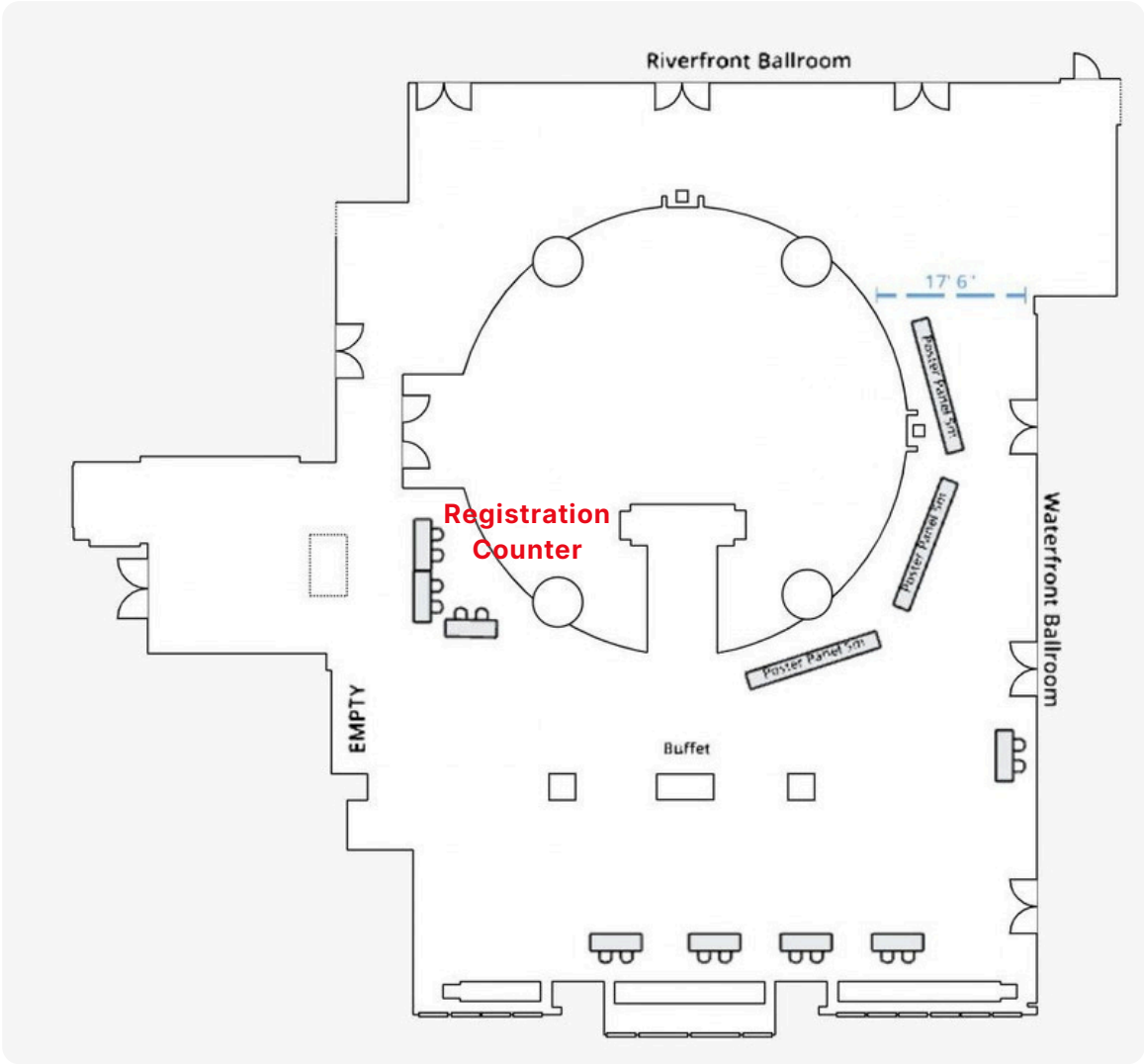
Travel Time: **~20-25 minutes**

- Download Grab, Gojek, or TADA from App Store / Google Play.
- Set your destination to: Grand Copthorne Waterfront Hotel Singapore
- Choose a service type (Budget, Standard, Premium, or 6-seater).

Pickup points are marked at each terminal.

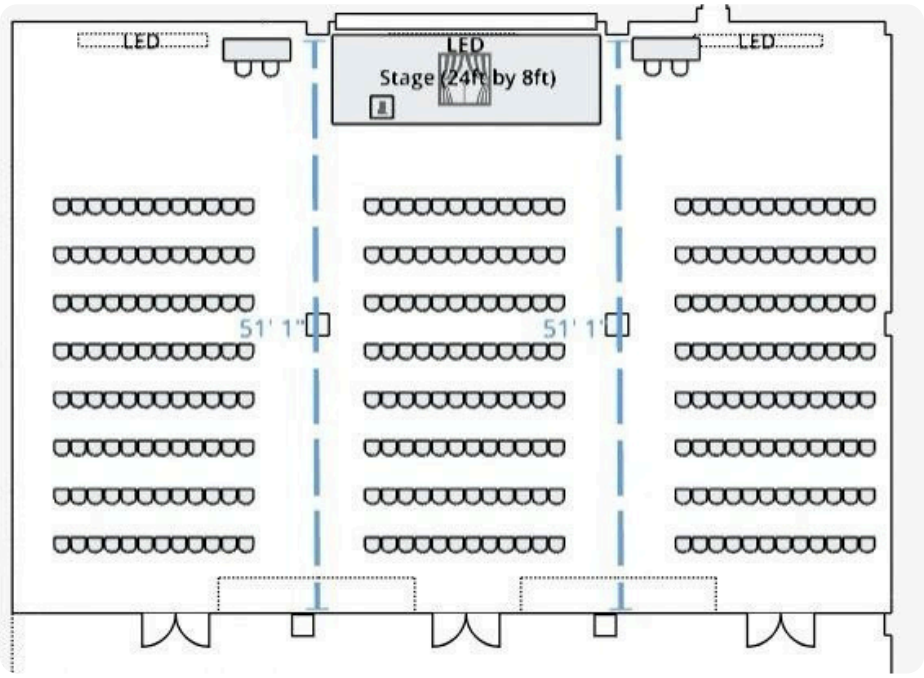
FLOOR PLAN

VENUE OVERVIEW

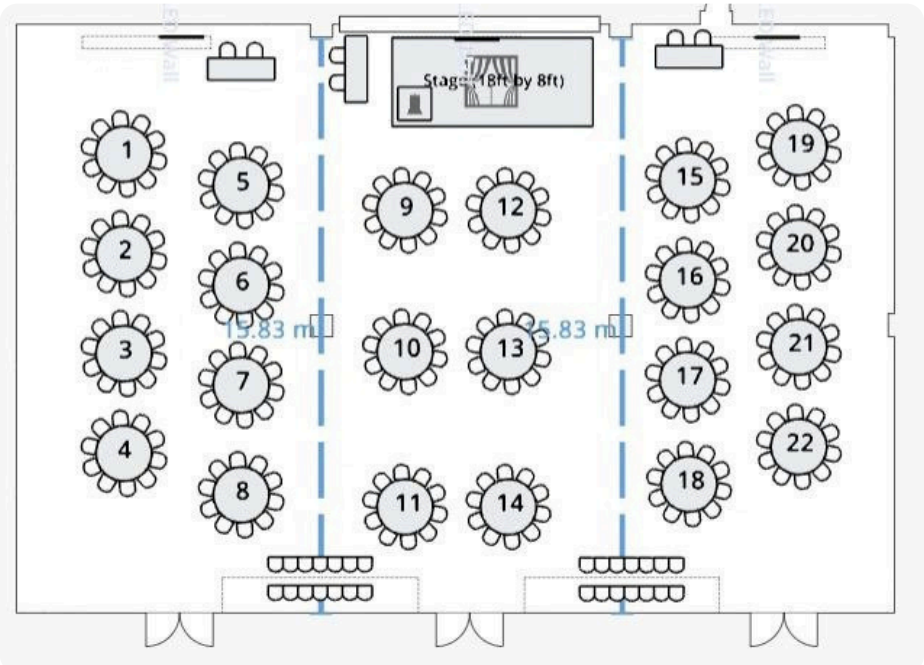


FLOOR PLAN

DAY 1 THEATRE: 280 pax + 24 x 8ft stage



FLOORPLAN FOR DAY 2-3



GUIDELINES

Oral Presentation

Speakers are requested to attend at least their own sessions from the beginning to the end. Session chairs may announce some information about their sessions.

For the Oral papers, the total presentation time is 10 minutes and 5 minutes for Q&As, The secretariat will provide a PC (MS Window 10; supports presentation format of Powerpoint or PDF files) in the Hall or respective breakout room. All presentations should be conducted using this PC.

It is recommended to prepare PDF format presentation files as backup in case there is any compatibility issue.

Poster Presentation

Poster boards will be prepared in portrait format with a maximum size of 85 cm (width) by 120 cm (height). Our recommendation for poster is A0 size (841mm * 1189mm) in Portrait Orientation.

Presenters are recommended to attach their posters by using Velcro tapes (which are available on-site). Do approach our Conference Assistant if you need any help.

Authors (or presenters) are expected:

1. To set up their posters start of the scheduled day.
2. To be presented with your poster during the poster session.
3. To explain your papers to the collected audience.
4. Remove your poster at the end of the day.

Security

Please ensure that you take your belongings with you at all times when leaving a room. Do not leave bags or laptops unattended.

AGENDA OVERVIEW

LECTURE SCHEDULE

Day 1

21 October, 2026 | Wednesday

Time	Activity	Venue
08:00 - 17:30	**Registration & Conference Kits Collection**	Foyer
08:30 - 08:35	**Opening and Welcome Speech by General Chair**	Waterfront Grand Ballroom
08:35 - 08:40	**Speech by TPC Chair**	Waterfront Grand Ballroom
08:40 - 09:20	**Keynote Speech 1: Prof Aaron Voon-Yew Thean**, National University of Singapore, Singapore	Waterfront Grand Ballroom
09:20 - 10:00	**Keynote Speech 2: Prof James C. M. Hwang**, Cornell University, Ithaca, New York (USA)	Waterfront Grand Ballroom
10:00 - 10:20	**Tea break**	
10:20-11:50	**(A1L-A) High Performance RF Building Blocks** (6 papers) Lecture 1 | Chr: **Miao Meng, Fanyi Meng** | Track: 1	Waterfront Ballroom 1
	(A1L-B) Advanced Memory for Compute, Search, and Intelligence (6 papers) Lecture 2 | Chr: **Longyang Lin, Hui Zhang** | Track: 4	Waterfront Ballroom 2
	(A1L-C) SS15.10: Advances in RFIC Design: Integrated Passive and Active Components for Next-Generation Systems (6 papers) Lecture 3 | Chr: **Forest Zhu** | Track: 15	Waterfront Ballroom 3
11:50 - 13:00	**Lunch + Poster session**	
13:00-14:30	**(A3L-A) Data Converter Techniques** (6 papers) Lecture 1 | Chr: **Moonhyung Jang, Mingqiang Guo** | Track: 2	Waterfront Ballroom 1
	(A3L-B) DC-DC Converters (6 papers) Lecture 2 | Chr: **Yingyi Yan, Junmin Jiang** | Track: 3	Waterfront Ballroom 2
	(A3L-C) SS15.11: Advanced Millimeter-Wave to Sub-THz Architecture, Circuits and Systems for Next-Generation Communication (6 papers) Lecture 3 | Chr: **Kenichi Okada, Chun Wang** | Track: 15	Waterfront Ballroom 3
14:35-15:55	**(A4L-A) SS15.21: Sensors, Sensing Circuits and Systems** (4 papers) Lecture 1 | Chr: **Jiang Wei** | Track: 15	Waterfront Ballroom 1
	(A4L-B) Chips and Systems for Intelligent Robot and Embodied AI (5 papers) Lecture 2 | Chr: **Haozhe Zhu, Mingyu Wang** | Track: 12	Waterfront Ballroom 2
	(A4L-C) SS15.6: Research Trends of RF Power Devices (5 papers) Lecture 3 | Chr: **Wen-Cheng Lai** | Track: 15	Waterfront Ballroom 3

AGENDA OVERVIEW

LECTURE SCHEDULE

Day 1

21 October, 2026 | Wednesday

Time	Activity	Venue
16:00-17:15	**(A5L-A)** **SS15.15: AI-Era Optical Interconnects: Electronic-Photonic Co-Design and integration** (5 papers) Lecture 1 | Chr: **Dan Li** | Track: 15	Waterfront Ballroom 1
	(A5L-B) **SS15.13: Power IC Technology for AI Data Centers** (5 papers) Lecture 2 | Chr: **Wai Tung Ng, Weijia Zhang** | Track: 15	Waterfront Ballroom 2
	(A5L-C) **SS15.2: Spintronics Computing and Logic** (3 papers) Lecture 3 | Chr: **Yan Zhou** | Track: 15	Waterfront Ballroom 3
17:15 - 17:40	**Tea break**	
17:40 - 18:30	**Panel Session**	Waterfront Grand Ballroom
18:30 - 21:00	**Welcome reception**	Waterfront Grand Ballroom

POSTER SCHEDULE

Day 1

21 October, 2026 | Wednesday

Time	Activity	Poster
11:50-13:00	**(A2P-D)** **RF Circuits** (2 papers) Chr: **Loo Xi Sung** | Track: 1	**P01**
	(A2P-E) **Processor and Chiplet Architectures** (2 papers) Chr: **Fengbin Tu, Xin Si** | Track: 4	**P02**
	(A2P-F) **High-Speed Wireline and Optical Circuits (poster)** (2 papers) Chr: **Fuzhan Chen, Xin Wang** | Track: 5	**P03**
	(A2P-H) **Chips and Systems for Intelligent Robot** (2 papers) Chr: **Zhuo Zou, Mingyu Wang** | Track: 12	**P05**
	(A2P-I) **AI for ICs** (3 papers) Chr: **Do Anh Tuan** | Track: 13	**P06**
	(A2P-J) **Micro-nano Optoelectronic Chips and Integrated Devices 1** (2 papers) Chr: **Weicong Na, Baolu Guan** | Track: 15	**P07**

AGENDA OVERVIEW

LECTURE SCHEDULE

Day 2

22 October, 2026 | Thursday

Time	Activity	Venue
08:00 - 17:30	Registration & Conference Kits Collection	Foyer
08:40 - 09:20	**Keynote Speech 3: CS Chua**, Infineon Technologies Asia Pacific Pte. Ltd., Singapore	Waterfront Grand Ballroom
09:20 - 10:00	**Keynote Speech 4: Chao Chen**, Suzhou Chuangjie Intelligent Technology Co., Ltd., China	Waterfront Grand Ballroom
10:00 - 10:20	**Tea break**	
10:20-11:50	**(B1L-A) Modeling, Simulation & Thermal Analysis** (6 papers) Lecture 1 | Chr: **Dr. Yichuan Bai** | Track: 8	Waterfront Ballroom 1
	(B1L-B) Packaging, Reliability, and Emerging Devices (6 papers) Lecture 2 | Chr: **Tao HANG, Faxing CHE** | Track: 10	Waterfront Ballroom 2
	(B1L-C) SS15.5:RF, Millimeter-Wave and Terahertz Integrated Circuits for Wireless Communication and Sensing (6 papers) Lecture 3 | Chr: **Keping Wang** | Track: 15	Waterfront Ballroom 3
11:50 - 13:00	**Lunch + Poster session**	
13:00-14:30	**(B3L-A) SS15.1: Breakthrough in Ultra-Broadband 5G/6G Communication Chips** (6 papers) Lecture 1 | Chr: **Fanyi Meng** | Track: 15	Waterfront Ballroom 1
	(B3L-B) AI Accelerators for DNN and Transformers (6 papers) Lecture 2 | Chr: **Aili Wang, Bo Wang** | Track: 13	Waterfront Ballroom 2
	(B3L-C) SS15.3: Communication, packaging and hybrid Integration in AI area: Theories, Algorithms, and Applications (6 papers) Lecture 3 | Chr: **Yujie Li** | Track: 15	Waterfront Ballroom 3
14:35-15:55	**(B4L-A) SPAD Imaging and Advanced Sensor Interfaces** (5 papers) Lecture 1 | Chr: **Hua Fan, Runjiang Dou** | Track: 7	Waterfront Ballroom 1
	(B4L-B) EH, WPT, and Gate Driver (5 papers) Lecture 2 | Chr: **Weijia Zhang, Dongfang Pan** | Track: 3	Waterfront Ballroom 2
	(B4L-C) RF Front-End and Frequency Generation (5 papers) Lecture 3 | Chr: **Yuncheng Zhang, Shiheng Yang** | Track: 1	Waterfront Ballroom 3

AGENDA OVERVIEW

LECTURE SCHEDULE

Day 2

22 October, 2026 | Thursday

Time	Activity	Venue
16:00-17:30	**(B5L-A)** **SS15.17: Next-Generation Wireless Technologies for Biomedical and IoT Applications** (6 papers) Lecture 1 | Chr: **Hyun-su Lee** | Track: 15	Waterfront Ballroom 1
	(B5L-B) **SS15.19: Compute-in-memory architectures, circuits and devices for next-generation AI systems** (6 papers) Lecture 2 | Chr: **Yuqi Su** | Track: 15	Waterfront Ballroom 2
	(B5L-C) **SS15.16: Domain-specific Hardware Design for Perception of UAVs, Humanoid Robots and Autonomous Vehicles** (6 papers) Lecture 3 | Chr: **Ye Liu** | Track: 15	Waterfront Ballroom 3
18:30 - 19:00	**Cocktail reception**	Foyer
19:00-22:00	**Banquet**	Waterfront Grand Ballroom

POSTER SCHEDULE

Day 2

22 October, 2026 | Thursday

Time	Activity	Venue
11:50-13:00	**(B2P-D)** **Analog Techniques and Power Management** (5 papers) Chr: **Yuan Gao, Yang Jiang** Track: 2	**P01**
	(B2P-F) **Biomedical ICs and Systems** (3 papers) Chr: **Sunwoo Lee** Track: 6	**P03**
	(B2P-G) **Thermal and Optical CMOS Sensing Systems** (2 papers) Chr: **Ka-Meng Lei** Track: 7	**P04**
	(B2P-H) **Emerging Memory Devices and Architectures** (4 papers) Chr: **Can Li** Track: 9	**P05**
	(B2P-I) **Emerging Device and Materials** (1 paper) Chr: **Chenxi Zhu, Jun WANG** Track: 11	**P06**
	(B2P-J) **Micro-nano Optoelectronic Chips and Integrated Devices 2** (1 paper) Chr: **Weicong Na, Baolu Guan** Track: 15	**P07**

AGENDA OVERVIEW

LECTURE SCHEDULE

Day 3

23 October, 2026 | Friday

Time	Activity	Venue
08:00-14:00	Registration & Conference Kits Collection	Foyer
08:30-10:00	**(C1L-A)** **In-memory Computing Devices** (6 papers) Lecture 1 | Chr: **Lin Bao, Zongwei Wang** | Track: 9	Waterfront Ballroom 1
	(C1L-B) **Design Automation and Optimization** (6 papers) Lecture 2 | Chr: **Prof. Jing Tian** | Track: 8	Waterfront Ballroom 2
	(C1L-C) **SS15.9: Evolving RF, mm-Wave, and THz Front-Ends for Next-Generation Sensing and Communication Systems** (6 papers) Lecture 3 | Chr: **Xiang Yi** | Track: 15	Waterfront Ballroom 3
10:00-10:10	**Tea break**	
10:10-11:40	**(C2L-A)** **Efficient Accelerators for AI and Cryptography** (6 papers) Lecture 1 | Chr: **Ye Liu, Chao Wang** | Track: 4	Waterfront Ballroom 1
	(C2L-B) **Domain Specific and AI Assisted ICs** (6 papers) Lecture 2 | Chr: **Lujie Peng, Tao Tang** | Track: 13	Waterfront Ballroom 2
	(C2L-C) **High-Speed Wireline and Optical Circuits** (6 papers) Lecture 3 | Chr: **Xin Wang, Fuzhan Chen** | Track: 5	Waterfront Ballroom 3
11:40-12:30	**Lunch**	
12:30-14:00	**(C4L-A)** **SS15.12: Advanced CMOS RF and mmWave Frond-end Circuits** (6 papers) Lecture 1 | Chr: **Fanyi Meng** | Track: 15	Waterfront Ballroom 1
	(C4L-B) **SS15.4: IC based modules, system integration and applications** (6 papers) Lecture 2 | Chr: **Hu Fang** | Track: 15	Waterfront Ballroom 2
	(C4L-C) **SS15.8: Energy-Efficient Circuits and Systems for Intelligent Sensing and Wireless Data/Energy transfer** (6 papers) Lecture 3 | Chr: **Atila Alvandpour** | Track: 15	Waterfront Ballroom 3
14:05-15:20	**(C5L-A)** **Emerging Semiconductor Devices** (5 papers) Lecture 1 | Chr: **Sunbin Deng** | Track: 9	Waterfront Ballroom 1
	(C5L-B) **Analog Circuit Techniques** (5 papers) Lecture 2 | Chr: **Yuan Gao, Yuxuan Luo** | Track: 2	Waterfront Ballroom 2
	(C5L-C) **SS15.14: Millimeter-Wave and Terahertz Signal Generation for Next-Generation Communications and Sensing** (5 papers) Lecture 3 | Chr: **Cheng Yong** | Track: 15	Waterfront Ballroom 3

AGENDA OVERVIEW

LECTURE SCHEDULE

Day 3

23 October, 2026 | Friday

Time	Activity	Venue
15:25-16:55	**(C6L-A)** **SS15.18: Advanced Power Delivery for AI Computing: System Architectures, Modeling, and Converter Innovations** (6 papers) Lecture 1 | Chr: **Zhiguo Tong** | Track: 15	Waterfront Ballroom 1
	(C6L-B) SPECIAL SESSION: OpenPDK - Global FOSS Scholar Platform Chr: **Wladek Grabinski, Fujiang Lin**	Waterfront Ballroom 2
	(C6L-C) **SS15.20: Innovative Circuits and Systems: From Sensing to Intelligent Computing** (6 papers) Lecture 3 | Chr: **Jerald Yoo** | Track: 15	Waterfront Ballroom 3

AGENDA OVERVIEW

SOCIAL PROGRAM

Day 4 24 October, 2026 | Saturday

The Albatross File Exhibition

Free admission, limited to 50 participants per session. Registration is required.

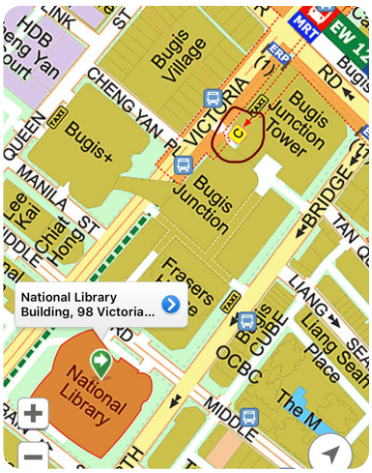


2 Sessions: Sesssion 1 - **9:50am** **OR** Sesssion 2 - **10:20am**

Meeting Venue: **Level 1 Lobby, National Library Building (NLB), 100 Victoria Street, Singapore 188064**

Directions:

Take the **East-West Line (Green Line)** to **Bugis MRT Station** and proceed via **Exit C**, as shown in the image below.



OPENING & WELCOME SPEECH BY CHAIR

Time: 0830 - 0835
Venue: Waterfront Grand Ballroom



Professor YEO Kiat Seng
General Chair, Organizing Committee of IEEE ICTA-2026

Tianjin University (TJU), China
Singapore University of Technology and Design (SUTD), Singapore

On behalf of the Organizing Committee, it is my pleasure to welcome all our Conference delegates and distinguished keynote speakers to the 9th IEEE Integrated Circuits, Technologies and Applications (IEEE ICTA-2026) at the green and beautiful island city of Singapore.

IEEE ICTA-2026 is organized by the National University of Singapore (NUS), Nanyang Technological University Singapore (NTU), Singapore University of Technology and Design (SUTD), Singapore Institute of Technology (SIT), Newcastle Australia Institute of Higher Education (NAIHE), Tianjin University (TJU), Tsinghua University (THU) and Agency for Science, Technology and Research (A*STAR). It is sponsored by IEEE Singapore Section and IEEE Solid-State Circuits Society (Singapore Chapter) as well as supported by Singapore Semiconductor Industry Association (SSIA), Asia-Pacific Science Technology Association (APSTA), Singapore Tourism Board (STB), National Innovation Center par Excellence (NICE) and Jiangsu Industrial Technology Research Institute (JITRI).

IEEE ICTA dates back to 2018 and is now recognized as one of the major international conferences in the highly important field of theory, design, and implementation of integrated circuits, systems and applications. The theme of ICTA-2026 is “Advancing IC with AI” to promote the use of artificial intelligence to automate, optimize, and accelerate chip development. The theme is timely in light of the increased design complexity, long chip development cycles, and high standards of quality and reliability demanded by the semiconductor industry.

The Conference provides a forum for IC designers, semiconductor manufacturing engineers and academics to share and discuss new R&D problems, ideas, techniques, results and applications in relation to integrated devices, circuits and systems. It offers a rich program of the highest quality with distinguished keynote and invited speakers from all over the world.

IEEE ICTA-2026 received more than 330 papers from North America, Europe, Asia and Oceania. These papers span from RF Circuits and Wireless Systems, Analog and Mixed-Signal ICs, Power Management ICs, Digital ICs and Memory, Wireline ICs, Biomedical ICs and Systems, Sensor ICs and Applications to EDA, Modeling, and Testing, Device and Process Technologies, Packaging and Hybrid Integration, Intelligent Robots, Emerging Technologies and Applications as well as ICs for AI and AI for ICs.

The authors of this Conference are invited to organize Special Issues or submit an extended version of their papers to Interdiscipline (www.elspub.com/journals/interdiscipline/home), Journal of Semiconductors (www.jos.ac.cn), and Integrated Circuits and Systems (ICAS) journal (www.qk.sjtu.edu.cn/ics).

Finally, I would like to take this opportunity to thank all members of the Organizing Committee for their tremendous effort, international advisors and steering committee members, distinguished keynote and invited speakers, sponsors and partners as well as participants for their continuing support to IEEE ICTA-2026, and to the Secretariat of this event for doing a fantastic job.

I wish all delegates a stimulating and fruitful time at the Conference, and an enjoyable stay in Singapore.

SPEECH BY TPC CHAIR

Time: 0835 - 0840
Venue: Waterfront Grand Ballroom



Professor LU Yan
Chair, Technical Program Committee of IEEE ICTA 2026

Tsinghua University, Beijing, China

First of all, I would like to take this opportunity to thank all the Technical Program Committee (TPC) Co-Chairs, Special Session Chair, Sub-committee Chairs/Co-Chairs, TPC Members, paper Authors and invited Speakers, for contributing to this great edition of IEEE International Conference on Integrated Circuits, Technologies & Applications (ICTA 2026). We received a record high number 330 of paper submissions, including 203 regular submissions and 127 special-session submissions. Therefore, ICTA 2026 has arrange about 220 lecture presentations and 31 posters, in a compact three-day full program.

Since its inaugural edition in Beijing in 2018, the IEEE ICTA conferences have been held successively in Chengdu, Nanjing, Zhuhai, Xi'an, Hefei, Hangzhou, and Macao. It has grown into one of the most influential high-level IEEE academic conferences in the field of integrated circuits in China. This year, the 9th ICTA conference marks a milestone: for the first time, ICTA is being held outside China, at the green and beautiful island city of Singapore, technically sponsored by IEEE Singapore Section and IEEE Solid-State Circuits Society (Singapore Chapter).

New this year, we added a new track of "ICs for AI and AI for ICs", in resonance with this year's theme "Advancing IC with AI", as artificial intelligence is in the midst of a historic surge. Many are calling 2026 the Common Era of AI, a turning point defined by a decisive shift from experimentation to infrastructure. AI is no longer a passive tool that answers questions or summarizes data; it has become an invisible, always-on utility and an active partner, woven into the core operations of organizations everywhere. Besides the papers in this new track, many works in the existing tracks are also designs for a faster, more energy-efficient, and stronger AI.

During the conference, the ICTA 2026 Best Papers will be selected from the sub-committee recommended papers, while the best papers awardees and also the candidates will be invited to submit extended full-length journal version to the Journal of Semiconductors (JOS), and the Integrated Circuits and Systems (ICAS) Journal. Also, the authors of this Conference are invited to organize Special Issues or submit an extended version of their papers to the journal Interdiscipline (www.elspub.com/journals/interdiscipline/home)

Last but not least, I would like to express my heartfelt gratitude to every member of the Organizing Committee, for their tremendous efforts in making ICTA 2026 an unforgettable experience. We sincerely hope every participant would enjoy this year's technical program and the days in Singapore, and also would forge new friendships and spark new ideas over the course of this international gathering.

KEYNOTE SPEAKERS

SPEAKER 1

Time: 0840 - 0920
Date: 21 October 2026 | Wednesday
Venue: Waterfront Grand Ballroom



Prof Aaron Voon-Yew Thean

National Univerisity of Singapore (NUS), Singapore

BIO:

Aaron Thean is the Globalfoundries Professor of Electrical and Computer Engineering at the National University of Singapore (NUS). He is also the Deputy President (Academic Affairs) and Provost at NUS. In addition to his administrative duties, he is also the Director of SHINE research center on Next-Generation Hybrid Electronics, where Heterogeneous Integration process and design are investigated to enable new system innovation by chip packaging and other additive processing. Prior to NUS, Aaron Thean was the Vice President of Logic Technologies at IMEC. Working with Semiconductor Industry leaders like Intel, TSMC, Samsung, Globalfoundries, Apple, and Sony, he directed the research and development of next-generation semiconductor technologies and emerging nano-device architectures. Prior to joining IMEC in 2011, he was with Qualcomm's CDMA technologies in San Diego, California. Aaron and his group worked on Qualcomm's 20nm and 16nm mobile System-On-Chip technologies. From 2007 to 2009, Aaron was with IBM, where he developed the 28-nm and 32-nm low-power bulk CMOS technology at IBM East Fishkill, New York. Aaron graduated from University of Illinois at Champaign-Urbana, USA, where he received his B.Sc. (Highest Honors), M.Sc., and Ph.D. degrees in Electrical Engineering (Edmund J. James Scholar). Recognised by Singapore's National Research Foundation (NRF) to be a NRF Returning Singaporean Scientist, he returned to Singapore to pursue his career as an academic in 2016. He has co-authored over 300 technical papers in the areas of advanced microelectronics and holds more than 50 US patents. He is fellow of the US National Academy of Inventors and IEEE.

Towards Chips that Rewire Themselves? How Novel Material-System Co-Design can Enable Them

ABSTRACT:

Ultra-low energy and area-efficient electronic systems are required to enable untethered computing at the edge of IoT. To realize self-learning edge-AI systems, conventional solely software-driven deep-learning neural networks becomes a major roadblock due the excessive energy expense of training. Hence, fundamental hardware change is likely needed. In this talk, we review our recent material innovations (E.g. Ferroelectric oxides and 2D Material) and we show how close coupling with new micro-architecture innovations (E.g. New memory physical layout and Monolithic 3D IC [1],[2](Fig.1(a)) may significantly accelerate in-memory computation. We explore wafer-level solution-processed CMOS-compatible use of 2D Material (MoS_2/WSe_2) [3](Fig.1(b)) to enable high-endurance memristors that can have properties superior to conventional oxide RRAMs. We discuss the use and enabling of multi-gated HZO-based low-thermal-budget ferroelectric oxide memory transistors for new reconfigurable non-volatile logic and interconnect [4] (Fig. 2(a)). In co-operation with specific system-level innovations, we review material-system co-design in data encoding for deep convolution neural network. We show through material-device-aware data encoding, error correction, and novel physical memory layout (staggered + Manhattan arrays) [1], that aim to simplify in-memory data processing, one can significantly manage variabilities while accelerating convolution deep neural network operations and offer substantial low-energy opportunities towards reconfigurable Edge-AI systems. Extending similar innovations to photonics, we show that new ferroelectric-lithium niobate integration can enable reconfigurable photonics and in-memory compute for photonics [5] (Fig. 2(b)).

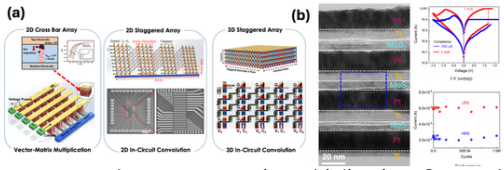


Fig. 1: (a) Left: Oxide ReRAM for in-memory analog vector-matrix multiplication, Center: Novel 2D stair-case ReRAM array to accelerate convolution computation for CNN [1], Right: a proposed 3D staggered array for high-throughput in-memory CNN computation [2]. (b) 3D-Stacked Analog ReRAM device with solution-processed MoS_2 switching layers [3].

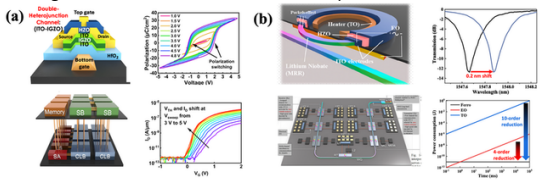


Fig. 2: (a) HZO-IGZO Dual-Gate Memtransistor and the transistor's non-volatile ferroelectric memory switching characteristics, with proposed application for BEOL-integrated switch matrix for non-volatile FPGA [4]. (b) HZO-Lithium Niobate Micro Ring Resonator (MRR), Electro-Optic Modulator and Memory with non-volatile photonic memory operations and energy reduction gains with respect to thermal-modulated MRR. We proposed it as a non-volatile switch for reconfigurable photonic inter-chip let interconnect system [5].

KEYNOTE SPEAKERS

SPEAKER 2

Time: 0920 - 1000
Date: 21 October 2026 | Wednesday
Venue: Waterfront Grand Ballroom



Prof James C. M. Hwang

Cornell University, Ithaca, New York (USA)

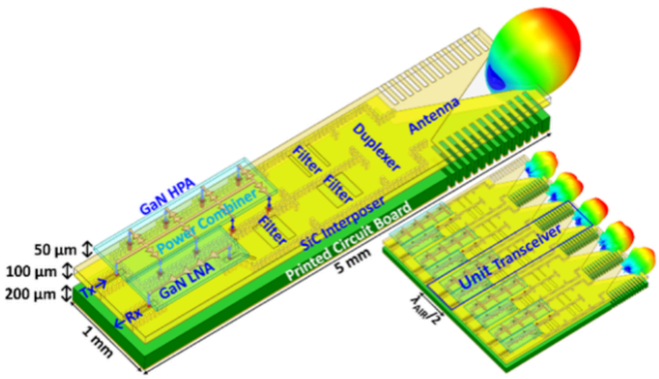
BIO:

James C. M. Hwang received the B.S. degree in physics from National Taiwan University, and the M.S. and Ph.D. degrees in materials science and engineering from Cornell University. He is currently a Professor at the Department of Materials Science and Engineering, Cornell University. Prior to that, he spent most of his academic career with Lehigh University, after years of industrial experience at IBM, Bell Labs, GE, and GAIN. He cofounded GAIN and QED; the latter became the public company IQE and remains the world's largest compound-semiconductor epitaxial wafer supplier. He was a Consultant for the U.S. Air Force Research Laboratory, and a Program Officer for GHz-THz Electronics with the Air Force Office of Scientific Research. He was an IEEE Distinguished Microwave Lecturer. He is an IEEE Life Fellow and an Editor of IEEE Journal of Microwaves. He has worked for decades on electronic, optoelectronic, and micro-electromechanical materials, devices, and circuits. He was the recipient of many honors and awards, including the IEEE Lester F. Eastman Award for outstanding achievement in high-performance semiconductor devices. His current research focuses on sub-THz materials, devices, and circuits for next-generation automobile radars, Internet of Space, and 6G wireless communications.

Heterogeneous Integrated Sub-THz Transceiver Frontend

ABSTRACT:

Heterogeneous integration of chiplets of different technologies on an interposer has been developed for digital and memory applications. Heterogenous integration for RF applications is just emerging. In this case, with few input/output channels, there is plenty of room in the bulk of the interposer for passives such as combiners, filters, duplexers, and antennas that are much more efficient than their thin-film counterparts. This makes it possible to have a complete RF frontend on an interposer. In particular, at millimeter-wave frequencies, substrate-integrated waveguides (SIWs) can have lower loss than microstrip or coplanar transmission lines. Further, with the signal fully enclosed in the SIW, transmit and receive channels can be placed next to each other without crosstalk. Thus, a linear phased array, with each transceiver narrower than a half wavelength, can be fabricated on the same interposer. In turn, the interposers can be stacked to form a 2D end-firing array. These points will be illustrated through the GaN-on-SiC technology. However, similar heterogeneous integration approaches are applicable to other device technologies and interposer materials.



PANEL SESSION

Time: 1740 - 1830
Date: 21 October 2026 | Wednesday
Venue: Waterfront Grand Ballroom

MODERATOR:



Dr Kok Chiang Liang

Associate Director (Research & Innovation), Newcastle Australia Institute of Higher Education

SPEAKERS:



Mr Victor Lye

Founder and CEO, SqSave



Prof Peter Lian Yong

Academician, York University's Lassonde School of Engineering



Prof James Hwang

Cornell University, Ithaca, New York, USA



Mr C. S. Chua

President and Managing Director, Infineon Technologies Asia Pacific Pte. Ltd., Singapore



Associate Professor Charles C.C. Lee

Director of the Centre for Sustainable Development, Newcastle Australia, (the Asia-Pacific hub of the University of Newcastle, Australia

KEYNOTE SPEAKERS

SPEAKER 3

Time: 0840 - 0920
Date: 22 October 2026 | Thursday
Venue: Waterfront Grand Ballroom



CS Chua
President and Managing Director
Infineon Technologies Asia Pacific Pte. Ltd., Singapore

BIO:

CS Chua is the Regional President of Asia Pacific of Infineon Technologies Asia Pacific Pte. Ltd. Based in Singapore, CS oversees the strategy in the region comprises of Australia, India, Indonesia, Malaysia, Philippines, Singapore, South Korea, Thailand and Vietnam with special focus on sales, marketing and distribution. He has held his current role since 2017.
CS has a Bachelor of Electrical and Electronics Engineering degree from the Nanyang Technological University in Singapore. He has been with Infineon since 2000.

Positions within and outside the company:

2017 | **President and Managing Director, Asia Pacific**
2008 | **Vice President, Automotive Regional Centre Asia Pacific**
2001 | **Manager, Automotive Marketing Asia Pacific**
2000 | **Product Marketing Manager, Industrial Microcontroller Global**
1998 | **Sales Unit Manager, PerkinElmer Optoelectronics**
1994 | **Senior Application Engineer, Motorola Semiconductor Products Sector**
1993 | **Development Engineer, Philips Consumer Electronics**

Membership of industry organisations and governing bodies:

Honorary Secretary (since 2023)
- Singapore Semiconductor Industry Association (SSIA)

Council Member (2018 – 2021)
- Singapore Manufacturing Federation (SMF)

L4/L5 Autonomous vehicles: requirements and challenges for ICs

ABSTRACT:

Advanced Driver Assistance Systems (ADAS) and Autonomous Driving (AD) technologies are reshaping the automotive industry, driven by increasing safety regulations, consumer expectations, and rapid progress in semiconductor and artificial intelligence capabilities. This keynote reviews current market trends across automation levels and analyzes segmentation from Level 1/2 (driver assistance) to Level 2+/3 (conditional automation) and Level 4/5 (high and full automation). While L1/L2 systems are now widely deployed, L2+/L3 solutions are expanding through enhanced perception and supervised autonomy, and L4/L5 development is accelerating in selected commercial and mobility applications.

We present an overview of modern ADAS/AD architectures, highlighting the transition from distributed electronic control units toward centralised and zonal computing platforms. Surround sensing technologies—including cameras, radars, lidars, and acoustic sensing—are examined as complementary modalities enabling robust environmental perception under diverse operating conditions. The increasing importance of multi-sensor fusion and AI-driven perception engines is discussed, emphasising scalability and real-time processing requirements.

This keynote further analyses the implications of centralised high-performance computing, including high-bandwidth data routing, in-vehicle networking, and optimized energy supply and power distribution. System-level constraints such as cybersecurity protection, functional safety compliance, redundancy strategies, and fail-operational design are addressed as critical enablers for higher automation levels.

Finally, we explore key requirements and challenges for integrated circuits (ICs) supporting ADAS/AD platforms, including computational density, power efficiency, thermal management, deterministic latency, safety certification, and long-term reliability. The convergence of sensing, computing, connectivity, and safety architectures demands highly integrated, scalable semiconductor solutions. This work provides a comprehensive perspective on architectural evolution and technology enablers shaping the next generation of intelligent vehicles.

- ADAS-AD general market trends
- ADAS-AD general architecture
- Market segmentation L1/L2, L2+/L3, L4/L5
- Surround Sensing Cameras, Radars, Lidars and Sound sensing
- Central computing, Sensor fusion, Zone, AI engines
- Data rounting & energy supply
- CyberSecurity, Functional safety, Redudancy
- ADAS-AD requirements and challenges for ICs

KEYNOTE SPEAKERS

SPEAKER 4

Time: 0920 - 1000
Date: 22 October 2026 | Thursday
Venue: Waterfront Grand Ballroom



Chao Chen (陈超)
General Manager & Shareholder
Suzhou Chuangjie Intelligent Technology Co., Ltd., China

BIO:

Chao Chen is General Manager of Suzhou Chuangjie Intelligent Technology Co., Ltd. and serves as Vice Chair of the Supercomputing and Intelligent Computing Committee of the China Computer Industry Association (CCIA). His career spans three distinct waves of computing: quantitative finance, AI infrastructure, and embodied intelligence.

Mr. Chen began his career in quantitative trading, where he built high-frequency computational systems in which microsecond-level latency directly translated to financial performance. This experience gave him a deep understanding of computing as a core production asset rather than an IT overhead.

He subsequently moved into the AI infrastructure space, building and operating large-scale intelligent computing centers equipped with tens of thousands of GPU accelerators. Through hands-on management of these facilities, he gained first-hand insight into the system-level challenges of thermal management, power delivery, and GPU utilization that define the economics of AI at scale.
Today, Mr. Chen is an active investor in the embodied AI sector. His portfolio includes LingShen Technology (灵生科技), a Tsinghua University-origin company developing universal brain platforms and full-size humanoid robots deployed in smart manufacturing, healthcare, and data center inspection; and TIEN Kung (天工), the Beijing Innovation Center of Humanoid Robotics backed by MIIT and the Beijing Municipality, known for pioneering open-source full-size humanoid robots with advanced whole-body dynamic control.

Through this unique combination of operational and investment experience — from optimizing compute in financial markets, to operating GPU clusters at national scale, to funding the robots that will carry AI into the physical world — Mr. Chen brings a practitioner's perspective on what the IC industry must deliver to enable the next generation of intelligent machines.

From Cloud to Edge: Building AI Computing Infrastructure for the Age of Embodied Intelligence

ABSTRACT:

The AI computing landscape is undergoing a fundamental shift — from centralized training to distributed inference, from data centers to robot bodies. This keynote draws on the speaker's multi-faceted experience as an operator of large-scale intelligent computing centers and an investor in embodied AI robotics companies to examine the full spectrum of AI computing challenges, from cloud to edge to on-body.

The talk begins with lessons from building and operating intelligent computing centers at scale, addressing the system-level challenges — thermal management, power supply, network interconnection, and GPU utilization — that determine infrastructure success or failure. It then pivots to the emerging frontier of embodied intelligence, drawing on insights from the speaker's investments in humanoid robotics, including LingShen Technology (a Tsinghua-origin embodied AI company) and TIEN Kung (China's national humanoid robot innovation platform). These ventures reveal an entirely new set of IC demands: extreme power efficiency under 50W, sub-10ms real-time inference latency, heterogeneous multi-modal processing, and safety-critical reliability — all within a mobile form factor.

The talk presents a three-tier computing architecture (cloud–edge–on-body) for embodied AI and concludes with actionable recommendations for the IC design community: how to bridge the gap between today's chips and the requirements of tomorrow's intelligent machines.

SPECIAL SESSIONS

*SESSION: **"OpenPDK - Global FOSS Scholar Platform"***
(C6L-B)

Time: 15:25-16:55
Date: 23 October 2026 | Friday
Venue: Waterfront Ballroom 2



GRABINSKI Wladek

GMC Consulting, Switzerland

BIO:

Wladek Grabinski received the Ph.D. degree from the Institute of Electron Technology, Warsaw, Poland, in 1991. From 1991 to 1998 he was a Research Assistant at the Integrated Systems Lab, ETHZ, Switzerland, supporting the CMOS and BiCMOS technology developments by electrical characterization of the processes and devices. From 1999 to 2000, he was with LEG, EPFL, and was engaged in the compact MOSFET model developments supporting numerical device simulation and parameter extraction. Later, he was a technical staff engineer at Motorola, and subsequently at Freescale Semiconductor, Geneva Modeling Center, Switzerland. He is now a consultant responsible for SPICE modeling, characterization and parameter extraction of MOST devices for the analog/RF IC applications. He is currently consulting on the development of next- generation compact models for the nanoscaled technology very large scale integration (VLSI) circuit simulation. His current research interests are in high-frequency characterization, compact modeling and its Verilog-A standardization as well as device numerical simulations of MOSFETs for analog/RF low power IC applications. He is an editor of the reference modeling book Transistor Level Modeling for Analog/RF IC Design and also authored or coauthored more than 50 papers. Wladek is the chair of the ESSDERC Track4: "Device and Circuit Compact Modeling" as well as has served as a member of organization committee of ESSDERC/ESSDERC, TPC of SBMicro, SISPAD, MIXDES Conferences; reviewer of the IEEE TED, IEEE MWCL, IJNM, MEE, MEJ. He is a Member At Large of Swiss IEEE ExCom and also supports the EPFL IEEE Student Branch acting as its Interim Branch Mentor. Wladek is involved in activities of the MOS-AK Association and serves as a coordinating manager since 1999.

ABSTRACT:

The semiconductor industry has been evolving and innovating for nearly a century, ever since the invention of the first transistor. This rapid growth is driven by the direct and proactive contribution of OpenSilicon CAD/EDA to the entire technology flow: from state-of-the-art semiconductor technologies and device-level compact/SPICE modeling to Verilog-A standardization and advanced IC designs for various high-tech applications. However, the semiconductor industry also faces significant challenges in sustaining a workforce of skilled technicians and engineers. To address the increasing global demand for well-trained talent, innovative pathways must be established to attract professionals and strengthen local microelectronics ecosystems. The OpenSilicon CAD/EDA platform, established using recently released OpenPDKs, provides a powerful new scholar framework to connect beginners, enthusiasts, and experienced mentors, allowing them to benefit from the fast-growing open-source IC design movement. Indeed, collaborative OpenSilicon IC design is increasingly viable due to the rapid growth of OpenPDKs offered by SkyWater, GF, ICsprout55, ToakiRikita, SCL and IHP. This talk highlights how the European Chips JU ODE4EC-AMS Project coordinates and strengthens Europe's OpenSilicon CAD/EDA ecosystem to advance SPICE/Verilog-A modeling and standardization, integrating a complete open-source IC design flow (Xschem, Qucs-S, ngspice, Xyce, OpenVAF, OpenEMS, Magic, KLayout, LibreLine), and showcasing representative analog/RF and digital IC design examples manufactured through this collaborative effort.

SPECIAL SESSIONS

*SESSION: **"OpenPDK - Global FOSS Scholar Platform"***
(C6L-B)

Time: 15:25-16:55
Date: 23 October 2026 | Friday
Venue: Waterfront Ballroom 2



Jun-ichi OKAMURA

AIST Solutions, OpenSUSI, Japan

BIO:

Jun-ichi OKAMURA began his career at Toshiba in 1986 as a DRAM memory designer and later worked at IBM in Burlington, Vermont, on alliance programs related to the first-generation DDR SDRAM.

In 1999, he joined THine Electronics as a lead SerDes designer in the fabless semiconductor business. In 2006, he founded Trigence Semiconductor, which received its first investment from Intel Capital in 2012. Unfortunately, due to the impact of the U.S.–China trade war, Trigence was unable to secure Series D funding and was legally liquidated in May 2022.

After being invited to the National Institute of Advanced Industrial Science and Technology (AIST) as a guest researcher, he joined AIST Solutions in June 2023, where he has been engaged in semiconductor ecosystem development and policy planning activities.
In April 2024, he became the Representative Director of OpenSUSI (Open Source Utilized Silicon Initiatives), where he promotes semiconductor design talent development and the growth of the open-source silicon ecosystem in Japan.

ABSTRACT:

Since October 2025, we have been publicly releasing the Tokai Rika 1 µm CMOS technology as an open-source PDK via the OpenSUSI repository. In this talk, I will first present the latest status of the open-source PDK development, including the key technical issues that have emerged and our ongoing efforts to refine and improve the overall methodology. I will then introduce the "First Tapeout" proposal in 2026 as a talent identification and development program. This initiative represents Japan's first attempt to provide hands-on experience covering the full RTL-to-GDSII-to-chip flow in collaboration with industrial partners. Finally, I will outline the OpenSUSI MPW shuttle program released for 2026, which aims to engage Japanese academia and further strengthen practical semiconductor design and fabrication experience.

SPECIAL SESSIONS

SESSION: ***"OpenPDK - Global FOSS Scholar Platform"***
(C6L-B)

Time: 15:25-16:55
Date: 23 October 2026 | Friday
Venue: Waterfront Ballroom 2



Ehrenfried SEEBACHER

ams-OSRAM AG, Austria

BIO:

Ehrenfried Seebacher is Senior Director of Research & Development at AMS-OSRAM, where he leads innovation activities in semiconductor technologies, design methodologies, and advanced product development. He has extensive experience in analog, mixed-signal, high-voltage, sensor, and automotive integrated circuits, spanning both semiconductor manufacturing and IC design environments. He is a Senior Member of the IEEE and has been actively involved in numerous European and international collaborative research projects, fostering cooperation between industry, universities, and research institutes. His work focuses on bridging academic innovation with industrial semiconductor development, including emerging topics such as compact modeling and process characterization, open-source EDA, open PDK enablement, design automation, and next-generation IC design methodologies.

Through his engagement with universities, EU-funded research initiatives, and international technology networks, he actively promotes knowledge exchange between academia and industry to accelerate innovation and strengthen Europe's semiconductor ecosystem.

ABSTRACT:

Open-source EDA tools and PDKs have become an important driver for semiconductor innovation, education, and collaborative research. While universities successfully utilize open-source ecosystems for teaching and prototyping, industrial semiconductor development requires significantly higher standards regarding analog/MS simulation, verification, qualification, reliability, IP protection, and sign-off quality.

This presentation provides an industrial perspective from ams-OSRAM on the adoption of open-source EDA technologies in professional IC development environments. We discuss the opportunities and limitations of current open-source analog and digital design flows, the challenges of integrating industrial PDKs, and the role of open-source tools as complementary solutions alongside established commercial EDA platforms.

The talk highlights practical experiences, industry-academia collaboration models, and a roadmap for leveraging open-source technologies to accelerate innovation, improve accessibility, and strengthen the resilience of semiconductor design ecosystems while maintaining industrial quality requirements.

SPECIAL SESSIONS

SESSION: ***"OpenPDK - Global FOSS Scholar Platform"***

(C6L-B)

Time: 15:25-16:55

Date: 23 October 2026 | Friday

Venue: Waterfront Ballroom 2



Dr. Da ZHANG

Zhejiang University/CTO, Zhejiang Chuangxin Integrated Process Platform, China

BIO:

Dr. Da Zhang is a Qiushi Distinguished Professor at the School of Integrated Circuits, Zhejiang University. He has long been engaged in R&D and productizations in the integrated circuit industry. Prior to joining Zhejiang University this year, Dr. Zhang served as an Executive Director at Synopsys in the United States, where his responsibilities include advanced node process co-development, sensor IP design, and silicon lifecycle management development. Before that, he accumulated years of valuable management and R&D experience at leading companies including AMD and Freescale, witnessing and contributing to key evolutions in the semiconductor industry. Dr. Zhang received his bachelor's and master's degrees from Zhejiang University and his Ph.D. from the University of Illinois at Urbana-Champaign. He holds 32 U.S. patents.

ABSTRACT:

Due to the high complexity and strong interdependence of integrated circuit (IC) design and manufacturing, new architectures and design concepts require comprehensive, systematic tape-out verification and iterative tuning in order to progressively reach product level maturity. However, the industry has long been constrained by closed PDK (Process Design Kit) ecosystems and high tape out costs, which have significantly hindered broad based innovation in the IC field.

This presentation introduces the pioneering work undertaken by Zhejiang University and the Chuangxin Integrated Circuit Process Platform in building an open source PDK/tape out ecosystem, as well as effective practices for empowering industrial innovation and development. Based on the newly established full scale 12 inch production line, the platform has developed high quality CMOS processes and is extending into various impactful specialty process domains. The process technologies developed by the platform are open to the public to empower the industry. In collaboration with the Institute of Computing Technology, Chinese Academy of Sciences, the platform has formed a full chain open source ecosystem encompassing design, IP, and PDK. This open source ecosystem strongly supports high quality talent development, novel concept validation, and large scale industrial enablement.

SPECIAL SESSIONS

*SESSION: **"OpenPDK - Global FOSS Scholar Platform"***
(C6L-B)

Time: 15:25-16:55
Date: 23 October 2026 | Friday
Venue: Waterfront Ballroom 2



Dr. Yutao MA

VP of R&D, Primarius Technologies. Ltd., China

BIO:

Dr. Yutao Ma received his bachelor's degree in 1996 and his Ph.D. in 2001, both in Microelectronics from Tsinghua University. He has since worked in the EDA industry for over 20 years, from Celestry to Cadence and then Primarius. His expertise includes semiconductor device modeling, circuit simulation, and yield analysis. Dr. Ma is currently Vice President of R&D at Primarius Technologies, where he leads technology innovation, new product development, and the R&D engineering infrastructure team. He also serves as Director of the EDA Innovation Key Laboratory of Shandong Province and Co-Director of the Primarius-Peking University DTCO Innovation Laboratory. Dr. Ma has published dozens of technical papers in leading journals and conferences and holds multiple patents in device modeling, simulation algorithms, yield analysis, and hardware acceleration.

ABSTRACT:

Advanced semiconductor technologies are transforming device characterization and modeling from model-delivery tasks into critical infrastructure for DTCO. This talk presents a "silicon-to-design" loop spanning multi-domain measurement, compact modeling, parameter extraction, model QA, and circuit simulation. Challenges in FinFET/GAA, RF, reliability, and dynamic-bias noise are discussed, together with how automation and AI can improve modeling efficiency under physics-based constraints and rigorous governance. Primarius' integrated capabilities in measurement, modeling, automated extraction, QA, and simulation are used to illustrate a practical path toward intelligent, learning-based model development for DTCO.

SPECIAL SESSIONS

*SESSION: **"OpenPDK - Global FOSS Scholar Platform"***
(C6L-B)

Time: 15:25-16:55
Date: 23 October 2026 | Friday
Venue: Waterfront Ballroom 2



Prof. Alex GU

National Innovation Center Par Excellence (NICE), China

BIO:

Prof. Alex Gu is a Vice President of the National Innovation Center Par Excellence (NICE), overseeing the MicroNano and Integrated Circuit Division, as well as the Overseas and Hong Kong/Macao/Taiwan Cooperation Department. Prior to his current post, Prof. Gu was the founding Dean of the School of Microelectronics at Shanghai University, the Deputy Executive Director of the Institute of Microelectronics (IME) Singapore, and a Principal Scientist at Honeywell International, Inc. (Minnesota, USA). Prof. Gu brings 20+ years of experience in R&D, Education, Management and Commercialization. Prof. Gu's research interest is in the field of Micro Electro Mechanical Systems (MEMS), primarily in Aluminum Nitride (AIN) – based functional thin films and related MEMS sensors. Prof. Gu is a class 1998 PhD alumni of the University of Minnesota.

ABSTRACT:

This report presents the strategic landscape and international cooperation opportunities for application-driven integrated circuit (IC) innovation in China's Yangtze River Delta, facilitated by the National Innovation Center par Excellence (NICE). Despite possessing the nation's most complete IC industrial chain, the region faces challenges including advanced process gaps, reliance on imported equipment, and insufficient industrial synergy. To address these, NICE operates a "Grant-to-Equity" model to de-risk early-stage ventures and focuses its R&D portfolio on a "Beyond Moore" strategy—encompassing wide-bandgap power devices, advanced packaging/Chiplet, silicon photonics, and MEMS—to build a distinctive specialty process and pilot-test supply chain driven by real-world applications in automotive, AI, and industrial sectors. Through case studies and a commitment to open global partnerships, NICE aims to bridge the gap between research and commercialization, overcome high-end technology bottlenecks, and co-build a resilient and collaborative innovation ecosystem with international partners.

SPECIAL SESSIONS

SESSION: ***"OpenPDK - Global FOSS Scholar Platform"***

(C6L-B)

Time: 15:25-16:55

Date: 23 October 2026 | Friday

Venue: Waterfront Ballroom 2



Dr. Alex ZHAO

Founder/CEO Zhuhai SiChip Technology Co., Ltd., China

BIO:

Dr. Zhao holds a PhD from the University of Southampton, UK, where he studied under Prof. Bashir Al-Hashimi, Fellow of the Royal Academy of Engineering. He began research on 2.5D/3D stacked-chip design in 2008 as a member of one of the world's earliest teams chip-architecture design methodologies.The team subsequently completed 3D-IC validation in collaboration with IMEC. With 15 years of dedicated experience in design and development, Dr. Zhao has published numerous papers at leading international venues and received the VLSI-SoC International Best Paper Award. He currently serves as Founder and Chief Scientist of Zhuhai SiChip Technology Co., Ltd., where he leads projects under China's National Key R&D Program and directs his team in the independent research and development of 2.5D/3D stacked-chipEDAsoftware, driving breakthroughs in the semiconductor industry through full-flow back-end EDA tools and solutions.

ABSTRACT:

By reconfiguring chip stacking and interconnect, 2.5D/3D IC technology overcomes the bottlenecks of conventional planar integration, but it also introduces unprecedented system complexity—spanning micro-bump pitch, through-silicon via (TSV) density, and—which steadily widens the gap between design and manufacturing process.

This presentation focuses on a new paradigm of System-Technology Co-Optimization (STCO) driven by the dual engines of "AI + EDA." First, we will analyze the coupling mechanisms between design rules and process windows in 2.5D/3D ICs,exposing the efficiency bottleneck inherent in the traditional serial design-process iteration model. , we will explore how large-scale AI models can empower the EDA toolchain to enable full-flow intelligence—from architecture exploration and place-and-route to package signoff, thereby achieving rapid convergence to optimal solutions within ultra-large search spaces. Finally, we will share practicalSTCO implementations in representative scenarios such as High Bandwidth Memory (HBM) and chiplet-based designs, demonstrating how early process-aware design optimization and manufacturability-driven architectural innovation can deliver systematic breakthroughs in PPPAC . We look forward to exploring the new frontiers of advanced packaging together with.

SPECIAL SESSIONS

*SESSION: **"OpenPDK - Global FOSS Scholar Platform"***
(C6L-B)

Time: 15:25-16:55
Date: 23 October 2026 | Friday
Venue: Waterfront Ballroom 2



Prof Fujiang LIN

University of Science and Technology of China (USTC), China

BIO:

Fujiang Lin，Professor at the University of Science and Technology of China (USTC); Former Vice Dean of the School of Microelectronics; Senior Consultant at the Jiangsu Industrial Technology Research Institute Innovation Centre.

Prof. Lin earned his bachelor's and master's degrees as a member of USTC's Class of 1977, followed by his doctoral degree in West Germany. Under Singapore's EDB Scheme, he relocated to Singapore in 1993. He has worked at numerous cross-border industrial, academic and research institutions and successfully founded the startup Transilica. In 2009, he was selected as a National Distinguished Innovative Talent and returned full-time to his alma mater USTC. He served as Executive Director of the 23rd Department and co-founded China's National Demonstrative School of Microelectronics. He has supervised nearly 200 graduate students, published more than 200 academic papers, and holds over 80 invention patents.

His primary research interests cover microwave technology, micro-nano device modeling, wireless communication chip design, and optoelectronic chip design, with more than 30 years of extensive international experience in industry-academia-research collaboration.

In the industrial sector, he previously served as an independent director of Shanghai Fudan Microelectronics Co., Ltd., and was the founder and Chairman of Jiangsu Kedahengxin Semiconductor Pte., Ltd., leading his team to develop electrical chips for optical communication.

Prof. Lin is a co-founder of two international IEEE conferences: IEEE RFIT and IEEE ICTA.

ABSTRACT:

Thirty-seven years ago, the speaker's doctoral dissertation in West Germany addressed the consistency issue of parameter extraction for microwave device modeling—a challenge that remains prevalent to this day. Upon completing his PhD, the speaker relocated to Singapore. He subsequently carried out pioneering research on modeling, parameter extraction and chip design for state-of-the-art semiconductor devices at several renowned cross-border institutions, including Singapore's Institute of Microelectronics (IME), the HP EEsof Semiconductor Modeling Center in Singapore, and the SPICE team of Chartered Semiconductor Manufacturing. His technical contributions enabled a one-pass success of an RF chip development project. Drawing on nearly four decades of experience in semiconductor device modeling, this talk will share practical modeling methodologies, persistent technical bottlenecks, and validated strategies for effective parameter extraction accumulated throughout his career. Also will share his effort to bring modeling activity in R10/R11 to align with the international compact model coalition.

LECTURE SESSION - DAY 1

Time: **10:20-11:50**
Date: **October 21, 2025, Wednesday**

Session - High Performance RF Building Blocks

Session Chair: **Miao Meng, Fanyi Meng**

Session code: **A1L-A**		
Venue: **Lecture 1 - Waterfront Ballroom 1**		
Paper ID	**Track**	**Paper Info.**
7328	1	**Title:** A Time-Mode-Doherty Digital Quadrature Power Amplifier Based on 2-Bit Delta-Sigma Modulator **Author:** **Duo Li, Yuncheng Zhang, Kenichi Okada**
7056	1	**Title:** A 24-42 GHz 6-Bit CMOS Hybrid Gain Controller with Integrated Attenuator and Phase-Reversal Variable Gain Amplifier for 5G NR FR2 Phased-Array Systems **Author:** **Xiangyang Luo, Tao Yuan, Hongtao Xu, Yun Yin**
7116	1	**Title:** A 24.5–42.0 GHz 7-Bit High-Precision and High-Gain Active Phase Shifter with Below 0.58° RMS Phase Error in 28-nm CMOS **Author:** **Xiangyang Luo, Tao Yuan, Hongtao Xu, Yun Yin**
7192	1	**Title:** A 10.1–17.6 GHz Multi-Band Driver Amplifier in 55-nm CMOS **Author:** **Shujie Li, Ziyi Liu, Dixian Zhao**
7195	1	**Title:** A 21.8~36.3 GHz Power Amplifier with Magnetically Coupled Resonator Achieving 21.6±1.5 dB Gain Flatness **Author:** **Bowei Feng, Yukun He, Pengfei Yu, Shuyao Zheng, Yufei Wang, Lexuan Teng, Xiaoyan Gui**
7268	15.20	***INVITED*** **Title:** Achieving High Gain in a Single-Stage Amplifier Through Complementary Transimpedance Boosting **Author:** **Kian Ann Ng**

Session - Advanced Memory for Compute, Search, and Intelligence

Session Chair: **Longyang Lin, Hui Zhang**

Session code: **A1L-B**		
Venue: **Lecture 2 - Waterfront Ballroom 2**		
Paper ID	**Track**	**Paper Info.**
7311	4	**Title:** An STT-MRAM-Based Nonvolatile CAM for Exact Hamming Distance Computation **Author:** **Shiheng Li, Humiao Li, Longyang Lin**
7277	4	***INVITED*** **Title:** A 28-nm 6T2C eDRAM-Based TCAM with Workload-Profile-Guided Staged Search for Edge Decision-Tree Inference **Author:** **Yang Lou, Jun Wu, Yuqi Su**

LECTURE SESSION - DAY 1

Time: **10:20-11:50**
Date: **October 21, 2025, Wednesday**

Session - Advanced Memory for Compute, Search, and Intelligence

Session Chair: **Longyang Lin, Hui Zhang**

Session code: **A1L-B**		
Venue: **Lecture 2 - Waterfront Ballroom 2**		
Paper ID	**Track**	**Paper Info.**
7137	4	**Title:** Uniform Polarization Switching in AlScN/AlN Ferroelectric Superlattices for Reliable Memories **Author:** **Ruiqing Wang, Wenxin Sun, Yazhou Hou, Xinghui Wang, Siying Zheng, Jiuren Zhou, Yan Liu, Yue Hao, Genquan Han**
7026	4	**Title:** CP²A-ERA: An Experience Replay Accelerator Based on a CIM-Friendly Probabilistic-Partitioning Algorithm **Author:** **Kunpeng Gao, Yifan Wang, Yufeng Xie**
7130	4	**Title:** A 28nm 49.2 TFLOPS/W MXFP4 9T-SRAM Digital Compute-in-Memory Macro with Weight Precomputation and Reuse for Edge-AI Devices **Author:** **Haitao Huang, Panpan Tan, Shuting Cai**
7300	4	**Title:** Self-Organizing ECC for Configurable Correction Capability in Voltage-Controlled MRAM **Author:** **Zhibing Yao, Jinghan Zhang, Hao Cai**

Session - SS15.10: Advances in RFIC Design: Integrated Passive and Active Components for Next-Generation Systems

Session Chair: **Forest Zhu**

Session code: **A1L-C**		
Venue: **Lecture 3 - Waterfront Ballroom 3**		
Paper ID	**Track**	**Paper Info.**
7070	15.10	**Title:** An Inductorless 0.1 – 7 GHz Wideband LNA Employing Symbiotic Noise Cancellation Technique **Author:** **Jack Kee Yong, Xi Sung Loo**
7071	15.10	**Title:** A Differential Active Phase Shifter with LC T-Bridge Topology for mm-Wave Applications **Author:** **Yancheng Jiang, Xi Sung Loo**
7196	15.10	***INVITED*** **Title:** Automated Synthesis of On-Chip Quasi-Reflectionless LPF with Flat-Group-Delay **Author:** **Tianqi Chen, Wei Huang, Xi Zhu**
7213	15.10	**Title:** Design of a Sub-Terahertz SiGe Power Amplifier with Single-First-Driver Four-Way Distribution and Balun-Assisted Zero-Degree Combining **Author:** **Yiting Zhang, Hai Ye, Zenglong Zhao, Nengxu Zhu, Kaixue Ma, Kiat Seng Yeo, Fanyi Meng**

LECTURE SESSION - DAY 1

Time: **10:20-11:50**
Date: **October 21, 2025, Wednesday**

Session - SS15.10: Advances in RFIC Design: Integrated Passive and Active Components for Next-Generation Systems

Session Chair: **Forest Zhu**

Session code: **A1L-C**		
Venue: **Lecture 3 - Waterfront Ballroom 3**		
Paper ID	**Track**	**Paper Info.**
7310	15.10	**Title:** Input-Absorptive Flat-Group-Delay RF Bandpass Filter with Phase-Shifting Capability in GaAs Technology **Author:** **Chen Liang, Li Yang, Wei Wei, Jin-Xu Xu, Roberto Gómez-García, Xiu Yin Zhang**
7134	15.10	**Title:** A 27-32 GHz 6-Bit Vector-Sum Phase Shifter with a Folded Coupled-Line Quadrature Coupler **Author:** **Nengxu Zhu, Hai Ye, Huiying Wu, Zenglong Zhao, Yiting Zhang, Kaixue Ma, Kiat Seng Yeo, Fanyi Meng**

Time: **13:00-14:30**
Date: **October 21, 2025, Wednesday**

Session - Data Converter Techniques

Session Chair: **Moonhyung Jang, Mingqiang Guo**

Session code: **A3L-A**		
Venue: **Lecture 1 - Waterfront Ballroom 1**		
Paper ID	**Track**	**Paper Info.**
7012	2	**Title:** A 10GS/s 8-Bit Time-Interleaved SAR ADC with Exponential Moving Average-Based Gain and Offset Calibration and Current-Controlled Bit-Distribution-Based Ping-Pong Comparator Offset Calibration **Author:** **Rui Gao, Chaoyang Zhang, Runqiao Wang, Yiwei Wen, Peng Luo, Yintang Yang, Maliang Liu**
7016	2	**Title:** A 12-Bit 3-GS/s Pipelined ADC with Preamplification Technique and Split-Input Inverter-Based Amplifier **Author:** **Shuoxiong Yang, Dejian Li, Fule Li, Xiao Zhou, Zhihua Wang**
7115	2	**Title:** A High-Efficiency Amplifier-Free 10-Bit 160-MS/s Pipeline-SAR ADC with Modified Monotonic Switching and Interstage Bit Transfer **Author:** **Juncheng Huang, Qingjie Wang, Nan Li, Xiangshui Miao, Xingsheng Wang**
7323	2	**Title:** A 71-dB DR 20-MHz Bandwidth Bandpass ΔΣ Modulator with Leapfrog Active-RC Resonators **Author:** **Runkun Li, Xiao Wang, Xin Sun, Kong-Pang Pun**

LECTURE SESSION - DAY 1

Time: **13:00-14:30**
Date: **October 21, 2025, Wednesday**

Session - Data Converter Techniques

Session Chair: **Moonhyung Jang, Mingqiang Guo**

Session code: **A3L-A**		
Venue: **Lecture 1 - Waterfront Ballroom 1**		
Paper ID	**Track**	**Paper Info.**
7326	2	**Title:** A Task-Aware Decimation Filter for Simultaneous Signal Reconstruction and Band-Power Feature Extraction in Near-Sensor Classification **Author:** **Siqi Zhang, Jiaju Lu, Wang Ling Goh, Yuan Gao**
7344	2	**Title:** Topology-Nonideality-Aware Neural-Network Calibration with Signal-State-Adaptive Gating for Dynamic Nonlinearity and Memory Effect in High-Speed ADCs **Author:** **Peizhe Li, Hao Zheng, Danfeng Zhai, Chixiao Chen**

Time: **13:00-14:30**
Date: **October 21, 2025, Wednesday**

Session - DC-DC Converters

Session Chair: **Yingyi Yan, Junmin Jiang**

Session code: **A3L-B**		
Venue: **Lecture 2 - Waterfront Ballroom 2**		
Paper ID	**Track**	**Paper Info.**
7302	3	**Title:** A 10-to-40 VCR Hybrid Boost Converter with a Capacitor-Cross-Connected Input Stage for Piezoelectric Actuators **Author:** **Huaiyu Li, Huicheng Chen, Junmin Jiang, Xun Liu**
7104	3	**Title:** A Wide-Range Hybrid Converter with Multi-Rail Outputs for Compact PoL Application **Author:** **Zhetao Ding, Zheyuan Fei, Wanyuan Qu**
7248	3	**Title:** A 21–33-V Input, 1-V Output Hybrid Buck Converter with Sub-1-mV Ripple for 5G NR LEO Power Delivery **Author:** **Junjie Wang, Guigang Cai**
7207	3	**Title:** A 60V Compact Peak-Current-Mode Buck Converter with High-Side PWM Comparator and Sense-FET-Based Current Sensor **Author:** **Bing Yuan, Wenpeng Su, Yubo Shao**
7080	3	**Title:** A Type-ABBA Dual-Path SIMO DC-DC Converter with Improved Transient Response **Author:** **Yang Li, Yan Lu**

LECTURE SESSION - DAY 1

Time: **13:00-14:30**
Date: **October 21, 2025, Wednesday**

Session - DC-DC Converters

Session Chair: **Yingyi Yan, Junmin Jiang**

Session code: **A3L-B**		
Venue: **Lecture 2 - Waterfront Ballroom 2**		
Paper ID	**Track**	**Paper Info.**
7163	3	**Title:** A Duty-Cycle-Matched Multiphase PWM Generator for High-Frequency DC-DC Converters **Author:** **Diyang Gu, Wanyuan Qu**

Time: **13:00-14:30**
Date: **October 21, 2025, Wednesday**

Session - S15.11: Advanced Millimeter-Wave to Sub-THz Architecture, Circuits and Systems for Next-Generation Communication

Session Chair: **Kenichi Okada, Chun Wang**

Session code: **A3L-C**		
Venue: **Lecture 3 - Waterfront Ballroom 3**		
Paper ID	**Track**	**Paper Info.**
7023	15.11	**Title:** Silicon-Based W-Band Phase-Array Transceivers for Wide-Coverage, High-Data-Rate Wireless Communications **Author:** **Jian Pang, Yifu Li**
7044	15.11	**Title:** A D-Band Dual-Polarized Phased-Array Transceiver in 65nm CMOS for 6G UE **Author:** **Yudai Yamazaki, Kenichi Okada**
7055	15.11	**Title:** InP-Based Circuits and Systems for 300-GHz Wireless Communications **Author:** **Ibrahim Abdo, Hiroshi Hamada, Teruo Jyo, Hiroyuki Takahashi**
7118	15.11	**Title:** Multi-Dimensional Evolution of Terahertz Active Phased Arrays: Architecture, Scale and Noise **Author:** **Yan Li, Cheng Wang**
7347	16	***INVITED*** **Title:** 300-GHz-Band Phased-Array Transceivers in 65nm CMOS (Invited) **Author:** **Chun Wang, Kenichi Okada**
7349	15.11	***** INVITED ***** **Title:** RF Fully Connected Network and Applications for Concurrent Multi-Beam Forming **Author:** **Ho-Jin Song, Seunghoon Lee**

LECTURE SESSION - DAY 1

Time: **14:35-15:55**
Date: **October 21, 2025, Wednesday**

Session - SS15.21:Sensors, Sensing Circuits and Systems

Session Chair: **Jiang Wei**

Session code: **A4L-A**		
Venue: **Lecture 1 - Waterfront Ballroom 1**		
Paper ID	**Track**	**Paper Info.**
7229	15.21	**Title:** Photonic-Electronic Hybrid In-Memory Computing **Author:** **Zefeng Xu**
7150	15.21	**Title:** Silicon Photonic Innovations for Enhanced FMCW LiDAR: Devices, Modules and Engines **Author:** **Jing Wang, Tianqi Song, Ningyu Zhang, Hongduan Fan, Yicheng Wang, Mengxi Cui, Wensheng Huang**
7147	15.21	***INVITED*** **Title:** SPAD with Hybrid Guard Ring for Dark Noise Suppression in Standard 40 nm CMOS Process **Author:** **Zecheng Gao, Xuanyu Qian, Yinglong Zhu, Wei Jiang**
7133	15.21	**Title:** A 64× Streaming Compression Circuit for Real-Time Readout of 240 × 320 SPAD Arrays Based on FPGA **Author:** **Yaoqi Bao, Zhuang Yan, Yuxuan Li, Dong Li, Chongyao Xu, Lichen Feng, Rui Ma, Zhangming Zhu**

Session - DC-DC Converters

Session Chair: **Haozhe Zhu, Mingyu Wang**

Session code: **A4L-B**		
Venue: **Lecture 2 - Waterfront Ballroom 2**		
Paper ID	**Track**	**Paper Info.**
7031	12	**Title:** CovBA: A High-Throughput FPGA Accelerator for Robust Backend Optimization in Robot Vision Systems **Author:** **Xiaorui Mo, Ling Zhou, Cheng Nian, Jiaying Peng, Jiaqi Zhang, Fasih Ud Din Farrukh, Debing Zhang, Chun Zhang**
7113	12	**Title:** A Reward-Modulated On-Chip Online Learning Neuromorphic Accelerator for Dexterous Hand Control **Author:** **Yifu Liang, Hengtan Zhang, Zeyu Wang, Caicai Luo, Yuhan He, Yi Zheng, Siheng Lei, Li-Rong Zheng, Zhuo Zou**
7242	12	**Title:** ElasticAct: An Elastic Streaming FPGA Accelerator for Efficient Robot Action Generation **Author:** **Junming Zhang, Feiyang Gao, Huajun Sun, Qinyan Zhang, Ming Zeng, Chenghong Zou, Hao Sun, Zongliang Huo, Xiangshui Mia...**

LECTURE SESSION - DAY 1

Time: **14:35-15:55**
Date: **October 21, 2025, Wednesday**

Session - DC-DC Converters

Session Chair: **Haozhe Zhu, Mingyu Wang**

Session code: **A4L-B**		
Venue: **Lecture 2 - Waterfront Ballroom 2**		
Paper ID	**Track**	**Paper Info.**
7221	12	**Title:** SAGP-PIM: A Subarray-Group-Parallel PIM Architecture for Accelerating GEMV in Robotic VLA Inference **Author:** **Chenzhou Ye, Xiaojie Li, Yicong Zhang, Haiqiu Huang, Zhiyi Yu, Mingyu Wang**
7049	12	**Title:** Mixed-Precision Inference of a 120B MoE LLM on a Single Edge FPGA **Author:** **Lianjie He, Yuxin Li, Jindong Li, Xiang Chen**

Session - SS15.6: Research Trends of RF Power Devices

Session Chair: **Wen-Cheng Lai**

Session code: **A4L-C**		
Venue: **Lecture 3 - Waterfront Ballroom 3**		
Paper ID	**Track**	**Paper Info.**
7042	15.6	***INVITED*** **Title:** Frequency Synthesizer with Capacitor Switching Filter for Frequency-Shift Compensation **Author:** **Wen-Cheng Lai, Chang-Chun Chang**
7283	15.6	***INVITED*** **Title:** Design Series-Tuned Quadrature Cross Coupled Voltage-Controlled Oscillator **Author:** **Wen-Cheng Lai, Sheng-Lyang Jang, Wei Hao Lee**
7032	15.6	***INVITED*** **Title:** Wide-Band and High-Gain Low-Noise Amplifier with Pole-Zero Engineered Colpitts Active Trap **Author:** **Wen-Cheng Lai, Jingchen Wang**
7198	15.22	**Title:** Quasi 2D Ruddlesden–Popper Phase Perovskites for Low-Threshold Vertical Cavity Surface Emitting Lasers **Author:** **Sunan Li, Shuai Huang, Yu Wang, Baolu Guan**
7046	15.22	**Title:** A Dual-Mode Image Sensor Readout Circuit for Low Photodiode Current **Author:** **Han Huang, Xiyue Zhang, Xu Liu, Weicong Na, Baolu Guan**

LECTURE SESSION - DAY 1

Time: **16:00-17:15**

Date: **October 21, 2025, Wednesday**

Session - SS15.15: AI-Era Optical Interconnects: Electronic-Photonic Co-Design and integration

Session Chair: **Dan Li**

Session code: **A5L-A**		
Venue: **Lecture 1 - Waterfront Ballroom 1**		
Paper ID	**Track**	**Paper Info.**
7161	15.15	***INVITED*** **Title:** CMOS Optical Receiver Scaling: From 112G to 224G with Optical–Electrical Co-Design **Author:** **Dan Li**
7361	15.15	**Title:** Silicon Photonics Heterogeneous Integration (Si-PHI) for Optical Interconnects **Author:** **Xianshu Luo**
7360	15.15	**Title:** Highly Integrated Optical I/O Chip Design **Author:** **Jingjing Dong, Qianli Ma, Yu Xiao, Wenjie Li**
7332	15.15	**Title:** Electronic IC and Package Co-Design for 400-Gb/s/Lane and Beyond Optical Interconnects **Author:** **Yuan Gao, Fuzhan Chen, Sajay Gourikutty, Jiaqi Wu, Jyoti Malik, San Sandra, Mihai Rotaru, Surya Bhattacharya**
7359	15.15	**Title:** Silicon Microring Interconnects for CPO and OIO: From Lab to Industry **Author:** **Binhao Wang**

Session - SS15.13: Power IC Technology for AI Data Centers

Session Chair: **Wai Tung Ng, Weijia Zhang**

Session code: **A5L-B**		
Venue: **Lecture 2 - Waterfront Ballroom 2**		
Paper ID	**Track**	**Paper Info.**
7030	15.13	**Title:** Ai for Power Magnetics: from Core-Loss Prediction to Transient Hysteresis Modeling **Author:** **Yingyi Yan**
7050	15.13	***INVITED*** **Title:** Switch Resistance Loss Analysis of Switched-Capacitor Converters Using Ladder Diagrams **Author:** **Wing-Hung Ki, Guozhen Chang**
7058	15.13	**Title:** Vertical GaN MOSFETs and M-BDS for AI Power Applications **Author:** **Chao Liu**
7060	15.13	**Title:** Design-Space Structure of Analog Integrated Circuits and its Implications for Automated Sizing **Author:** **Han Wu, Chen Hu, Mo Huang, Yan Lu, Junmin Jiang**
7065	15.13	**Title:** GaN Power IC Technology for AI Data Centers **Author:** **Jin Wei, Junjie Yang, Teng Li, Jingjing Yu, Jiawei Cui, Meng Zhang**

LECTURE SESSION - DAY 1

Time: **16:00-17:15**
Date: **October 21, 2025, Wednesday**

Session - SS15.2: Spintronics Computing and Logic

Session Chair: **Yan Zhoui**

Session code: **A5L-C**		
Venue: **Lecture 3 - Waterfront Ballroom 3**		
Paper ID	**Track**	**Paper Info.**
7354	15.2	**Title:** Spintronic Probabilistic Computing for Hardware-Efficient Optimization Photo **Author:** **Yan Zhou**
7353	15.2	**Title:** Ultrafast Magnetism by Light Towards Ultrafast Switching of a Spintronic Device **Author:** **Bo Liu**
7352	15.2	**Title:** Fast Current-Driven Domain-Wall and Skyrmion Logic **Author:** **ZHAOCHU LUO**

LECTURE SESSION - DAY 2

Time: **10:20-11:50**
Date: **October 22, 2025, Thursday**

Session - Modeling, Simulation & Thermal Analysis

Session Chair: **Dr. Yichuan Bai**

Session code: **B1L-A**		
Venue: **Lecture 1 - Waterfront Ballroom 1**		
Paper ID	**Track**	**Paper Info.**
7145	8	**Title:** U-FNO-Assisted NEGF Simulation and Design Exploration of Two-Dimensional Material FETs **Author:** **Zekai Zhou, Shuo Zhang, Rui Ma, Qi Shen, Peng Zhang, Wen-Yan Yin**
7274	8	**Title:** Physics-Guided Automated Local Mesh Generation from Pre-Annealing Dopant Fields for TCAD Process Simulation **Author:** **Rui Ma, Shuo Zhang, Wenzhang Fang**
7027	8	**Title:** A Supply-Aware Model for Fast Transient Response Prediction of High-Speed Multi-I/O Links **Author:** **Wen-Tao Zhang, Peng Zhang, Xiang Wang, Jun Liu, Wen-Sheng Zhao**
7284	8	**Title:** Multi-Branch Frequency Enhanced ConvLSTM for Fast Transient Chip Temperature Field Prediction **Author:** **Zhangyin Gong, Jun Wang**
7337	8	**Title:** Neural Network-Based Compact Thermal Modeling of Photonic Integrated Circuits **Author:** **Kexin Zhu, Qing He**
-	-	*** INVITED *** **Title:** High Performance Harmonic-Shaping RF Oscillator Design: From Room Temperature to Cryogenic Applications **Author:** **Yatao Peng**

Session - Packaging, Reliability, and Emerging Devices

Session Chair: **Tao HANG, Faxing CHE**

Session code: **B1L-B**		
Venue: **Lecture 2 - Waterfront Ballroom 2**		
Paper ID	**Track**	**Paper Info.**
7120	10	**Title:** Thermal Management of a 6-Tier 3D Stacked DRAM-on-Logic Architecture **Author:** **Qiong Zhan, Hang Yan, Beibei Sheng, Jun Zhou, Peng Sun, Jia Chen, Yi Li**
7234	10	***INVITED*** **Title:** Substrate Warpage Prediction Using a Layerwise Stress Additive Residual Network and Evidence-Gated Calibration **Author:** **Yan Zhou, Yanyan Hu, Yu Yao, Jun Wang**

LECTURE SESSION - DAY 2

Time: **10:20-11:50**
Date: **October 22, 2025, Thursday**

Session - Packaging, Reliability, and Emerging Devices

Session Chair: **Tao HANG, Faxing CHE**

Session code: **B1L-B**		
Venue: **Lecture 2 - Waterfront Ballroom 2**		
Paper ID	**Track**	**Paper Info.**
7340	10	**Title:** Simulated and Measured 110–170-GHz TGV-Based Single-Sided GCPW-to-SIW Transition on 200-μm Glass **Author: Zhaoying Li, Pengran Yang, Kaiyue Liu, Yanqin Jin, Xiue Bao, Lianggong Wen**
7243	10	**Title:** Forward Alternating Current Electrodeposition for Regulating Grain Boundaries in Copper Coatings **Author: Jiazhi Chen, Peixin Chen, Longsheng Fang, Chuang Jiang, Li Ma, Hongqi Sun, Ming Li, Tao Hang**
7129	11	**Title:** Interface Engineering of AlScN Ferroelectric Devices via NH_3-Plasma-Treated TiN Electrodes **Author: Siying Zheng, Bochang Li, Jiuren Zhou, Xuefeng Yang, Bing Chen, Haiwen Xu, Yan Liu, Yue Hao, Genquan Han**
7189	15.22	***INVITED*** **Title:** Single-Mode MEMS-VCSEL with Gaussian Beam and Stable Divergence Angle Enabled by Metal Aperture Structure **Author: Baolu Guan, Jisheng Wang, Ning Cui, Hongzhuo Wang**

Session - SS15.5:RF, Millimeter-Wave and Terahertz Integrated Circuits for Wireless Communication and Sensing

Session Chair: **Keping Wang**

Session code: **B1L-C**		
Venue: **Lecture 3 - Waterfront Ballroom 3**		
Paper ID	**Track**	**Paper Info.**
7108	15.5	**Title:** A 12-Bit Digital Power Amplifier with IQ-Shared Logic and Three-Coupled-Transformer Achieving -28.3 dB EVM for 20 MHz 64-QAM **Author: Linhao Ma, Zongle Ma, Qing Li, Kaixue Ma, Keping Wang**
7109	15.5	**Title:** A 65 μW Efficient Circular-Memory Switched-Capacitor AFIR Baseband Filter for Low-Power Wireless Receivers **Author: Yicheng Chen, Zongle Ma, Linhao Ma, Qing Li, Keping Wang**
7135	15.5	**Title:** A 2.1-to-2.8-GHz 40.9-dBm GaN HEMT Power Amplifier with Lumped Dual-Harmonic Impedance Control **Author: Ke Liu, Xijun Huang, Zhicong Ye, Jing Xiao, Kai Tang**
7202	15.5	**Title:** A 5.6–10.7-GHz, 3.19 mW, 2.1dB NF Transformer-Based LNA with Gm-Boosting in 28 nm CMOS **Author: Liwei Zhao, Peiqi Jin, Qiang Guo, Yi Tang, Zhe Liu**

LECTURE SESSION - DAY 2

Time: **10:20-11:50**
Date: **October 22, 2025, Thursday**

Session - SS15.5:RF, Millimeter-Wave and Terahertz Integrated Circuits for Wireless Communication and Sensing

Session Chair: **Keping Wang**

Session code: **B1L-C**		
Venue: **Lecture 3 - Waterfront Ballroom 3**		
Paper ID	**Track**	**Paper Info.**
7211	15.5	**Title:** High-Resolution Imaging at 2.58 THz Using Power-Free Diode Detectors in 55-nm CMOS **Author: Fengyuan Zhang, Xin Zhang, Ningning Yan, Kaixue Ma**
7149	15.5	**Title:** A 0.4-to-1-GHz 12-Phase Injection-Locked Ring Oscillator with an Automatic Frequency Calibration Loop **Author: Qing Li, Linhao Ma, Zongle Ma, Kaixue Ma, Keping Wang**

Time: **13:00-14:30**
Date: **October 22, 2025, Thursday**

Session - SS15.1: Breakthrough in Ultra-Broadband 5G/6G Communication Chips

Session Chair: **Fanyi Meng**

Session code: **B3L-A**		
Venue: **Lecture 1 - Waterfront Ballroom 1**		
Paper ID	**Track**	**Paper Info.**
7018	15.1	**Title:** A Low-Noise Variable-Gain Amplifier with Low Gain Error for W-Band Phased Arrays in 130-nm SiGe BiCMOS Technology **Author: Zenglong Zhao, Nengxu Zhu, Hai Ye, Yiting Zhang, Kaixue Ma, Kiat Seng Yeo, Fanyi Meng**
7141	15.1	***INVITED*** **Title:** An Ultra-Wideband Passive Vector Synthesis Phase Shifter with Hybrid TC-RC Quadrature Generator for C/X/Ku/K-Band Applications **Author: Hai Ye, Sijia Bai, Yiting Zhang, Nengxu Zhu, Zenglong Zhao, Fanyi Meng, Kaixue Ma, Kiat Seng Yeo**
7182	15.1	**Title:** A Broadband Bidirectional Analog Baseband Chain for High-Speed Transceivers **Author: Ziyun Wu, Yuwen Long, Zongyang Zhang, Zhijian Chen, Guangyin Feng**
7197	15.1	***INVITED*** **Title:** Automated EM-Aware Synthesis of On-Chip Lumped-Element Broadband Quasi-Reflectionless Bandpass Filter **Author: Tianqi Chen, Wei Huang, Fanyi Meng, Xi Zhu**

LECTURE SESSION - DAY 2

Time: **13:00-14:30**
Date: **October 22, 2025, Thursday**

Session - SS15.1: Breakthrough in Ultra-Broadband 5G/6G Communication Chips

Session Chair: **Fanyi Meng**

Session code: **B3L-A**		
Venue: **Lecture 1 - Waterfront Ballroom 1**		
Paper ID	**Track**	**Paper Info.**
7210	15.1	**Title:** A 9.09–10.33-GHz Pole-Converged SR-VCO with Magnetic Feedforward and Implicit Common-Mode Noise Cancellation **Author:** **Qinwen Tong, Hao Shi, Xin Zhang, Kaixue Ma**
7220	15.1	**Title:** Low-Power Readout Circuit with a 14.6-Bit Delta-Sigma Modulator for Terahertz Imaging Systems **Author:** **Pengfei Ma, Yihan Wu, Xin Zhang, Fengyuan Zhang, Ningning Yan, Kaixue Ma**

Session - AI Accelerators for DNN and Transformers

Session Chair: **Aili Wang, Bo Wang**

Session code: **B3L-B**		
Venue: **Lecture 2 - Waterfront Ballroom 2**		
Paper ID	**Track**	**Paper Info.**
7288	13	**Title:** FlexBit: A Runtime-Reconfigurable Multi-Precision Accelerator for On-Device LLM Inference **Author:** **Ramesh Fernando, Mohamed Mukhtar, Anh Tuan Do, Bo Wang**
7167	13	**Title:** LACIA: An Incremental Sparse Attention Accelerator for Video Diffusion Transformers **Author:** **Jiaming Lin, Bo Hu, Xinyang Chen, Peng Zheng, Shun Zhang, Yu Gong, Hao Cai, Bo Liu**
7338	13	**Title:** A Unified Inner-/Outer-Product Matrix Accelerator with Shape-Aware Dataflow Selection **Author:** **Jialong Wang, Zhenhao Wang, Jinjing Bao, Mingde Duan, Cheng Zhang, Yingjie Zhao, Shirui Zhao, Hualian Tang, Xiguang W...**
7264	13	**Title:** EB-KVC: A High-Fidelity Entropy Budgeting Engine for KV Cache Management on LPU **Author:** **Jinghan Zhou, Zheng Wang, Xu Liu**
7045	13	**Title:** Bit-Level-Sparsity-Aware Adaptive Unstructured Pruning for DNN Acceleration **Author:** **Yuanmiao Lin, Peng Zhang, Ruidian Zhan, Xianghong Hu, Shuting Cai, Xiaoming Xiong**
7079	13	**Title:** A Bank-Aware Token Compaction Engine for Merge-and-Prune Sparse Vision Transformer Inference **Author:** **Hefei Feng, Ao Li, Fuchuan Luo, Zhisong Wei, Junbo Zhang, Hongxuan Guo**

LECTURE SESSION - DAY 2

Time: **13:00-14:30**
Date: **October 22, 2025, Thursday**

Session - SS15.3: Communication, packaging and hybrid Integration in AI area: Theories, Algorithms, and Applications

Session Chair: **Yujie Li**

Session code: **B3L-C**		
Venue: **Lecture 3 - Waterfront Ballroom 3**		
Paper ID	**Track**	**Paper Info.**
7186	15.3	**Title:** High-Speed Vertical Interconnect Design and Performance Evaluation of LTCC Interposer for 2.5D Optoelectronic Integration **Author: Jiaxin Zheng, Jianyu Shi, Jie Shi, Yang Yang, Shuo Jiang, Chi Zhang, Hao Wu, Yan Zhou, Jun Qin**
7224	15.3	***INVITED*** **Title:** A Programmable Ring-Oscillator Ising Processor on FPGA for Conditional Image Generation with Restricted Boltzmann Machines **Author: Zhekai Song, Zhihuai Zhang, Yudi Zhao, Yujun Wang, Shisheng Xiong, Kai Zhao**
7228	15.3	**Title:** An Output-Sensitive PL-PS Co-Design Architecture for High-Resolution YOLO Deployment on FPGA SoCs **Author: Ze Shi, Yudi Zhao, Jian Mei, Qiang He, Zhixing Zhao, Jixiang Wan, Kai Zhao**
7174	15.3	**Title:** Design and Optimization of Broadband High-Speed Interconnect Transmission Structure on LTCC/HTCC SiP **Author: Zhensong Li, Liang Zhang, Weixin Li, Kai Zhao**
7158	15.3	**Title:** A Low-Latency Dual-Path Compensated Serial Processing Element for Broadcast-Fed FPGA CNN Arrays **Author: Yujun Wang, Yudi Zhao, Qiang He, Kai Zhao**
7152	15.3	***INVITED*** **Title:** SpCA: Spectral Channel Attention Network for Spacecraft Telemetry Anomaly Detection **Author: Yuxin Zhang, Yujie Li, Mengyao Jin, Xingsheng Yu, Shuge Zhao, Shanbao He**

LECTURE SESSION - DAY 2

Time: **14:35-15:55**
Date: **October 22, 2025, Thursday**

Session - SPAD Imaging and Advanced Sensor Interfaces

Session Chair: **Hua Fan, Runjiang Dou**

Session code: **B4L-A**		
Venue: **Lecture 1 - Waterfront Ballroom 1**		
Paper ID	**Track**	**Paper Info.**
7169	7	**Title:** A Memory-Efficient Gated-SPAD Processing Architecture with On-Chip Sub-Gate Depth Extraction **Author:** **Rui Zhang, Zichen Song, Runjiang Dou, Xu Yang, Zhe Wang, Peng Feng, Jian Liu, Nanjian Wu, Liyuan Liu**
7175	7	**Title:** A Spiking-Reservoir CIC Preprocessor for Edge Grayscale Reconstruction in High-Speed SPAD Imaging System **Author:** **Zichen Song, Runjiang Dou, Rui Zhang, Zhe Wang, Xu Yang, Peng Feng, Jian Liu, Nanjian Wu, Liyuan Liu**
7216	7	**Title:** A Programmable-Gain Chopped Transimpedance Amplifier for Biomedical Optoelectronic Detection **Author:** **Yuxin Cai, Xiaojie Fang, Dan Shi, Ka-Meng Lei**
7335	7	**Title:** A 0.5-1.8 V Supply-Independent Capacitance-to-Digital Converter for Energy-Harvesting IoT Systems **Author:** **Tangzi Wu, Zhenyu Guo, Zihan Qin, Ruizhi Liu, Jiamin Li**
7261	7	**Title:** A Wide Dynamic Range and Low-Noise Analog Front-End for Neural Signal Acquisition in Brain-Computer Interfaces **Author:** **Lidan Zhang, Guoyi Yu, Weitao Yuan, Xiaohang Wang, Yiwei Dai, Weilin Chen, Jia Chen, Han Jia**

LECTURE SESSION - DAY 2

Time: **14:35-15:55**
Date: **October 22, 2025, Thursday**

Session - EH, WPT, and Gate Driver

Session Chair: **Weijia Zhang, Dongfang Pan**

Session code: **B4L-B**		
Venue: **Lecture 2 - Waterfront Ballroom 2**		
Paper ID	**Track**	**Paper Info.**
7257	3	**Title:** A 6.78-MHz 20-W 96.2%-Peak-Efficiency Single-Stage Wireless Power Receiver with an Efficient Driver-Supply Generating Technique **Author:** **Junfei Ge, Dongfang Pan, Lin Cheng**
7345	3	**Title:** A Scalable Multi-Input Piezoelectric Array Energy Harvesting Circuit with Arbitrary Phase Offset and Flying Capacitor Sharing **Author:** **Yikun Liu, Shousheng Han, Yuhui Shu, Yuhan Wang, Dan Xie, Xiaoming Wu, Xiaosen Liu, Yan Lu, Tian-Ling Ren**
7166	3	**Title:** A Fully Integrated Phase-Interleaved High-Density Inverting Charge Pump for Wearable LCD Display **Author:** **Wei Li, Chen Hu, Tiantian Tang, Xingyuan Li, Pishu Liang, Tianping Sun, Jianchao Xu, Junmin Jiang**
7313	3	**Title:** A Half-Bridge GaN Driver with On-Chip CISS-Variation Sensing for Device Health Monitoring **Author:** **Xiaoyu Wang, Hangxiao Ma, Qiaobo Ma, Yang Jiang, Rui P. Martins, Pui-In Mak**
7239	3	**Title:** A Power-to-Voltage Converter-Based MPPT Boost Converter for Micro Energy Harvesting **Author:** **Youlin Wu, Chenchang Zhan**

LECTURE SESSION - DAY 2

Time: **14:35-15:55**
Date: **October 22, 2025, Thursday**

Session - RF Front-End and Frequency Generation

Session Chair: **Yuncheng Zhang, Shiheng Yang**

Session code: **B4L-C**		
Venue: **Lecture 3 - Waterfront Ballroom 3**		
Paper ID	**Track**	**Paper Info.**
7289	1	**Title:** A 0.3-to-42GHz CMOS Receiver Supporting Full-Band Analog Phase Sensing Assisted Quadrature Error Calibration with 40-dB-IRR Enabling 1024-QAM Modulation **Author:** **Yichi Sun, Dongze Li, Jinglin Zhang, Wenjing Ye, Haikun Jia, Wei Deng, Rui Wu, Liangjiang Zhou**
7170	1	**Title:** A 0.022-mm² Ring VCO-Based Injection-Locked-Clock-Multiplier with Current-Isolated Delay Cells Achieving 247-fs RMS Jitter **Author:** **Zhaoshan Gao, Yu Lv, Zitao Hu, Dandan Zhao, Jiaxin Sun, Meng Ning, Runchen Wang, Ya Zhao, Chao Fan**
7321	1	**Title:** A 37-GHz-Bandwidth D-Band CMOS Receiver with a Sub-Harmonic Mixer Based on LO Power Regulation **Author:** **Yuchi Liu, Xiao Liu, Li Du, Jiacheng Guo, Yuan Du**
7041	1	**Title:** A D-Band Up-Conversion Sub-Harmonic Mixer with Simplified LO Scheme in 28nm CMOS **Author:** **Xiao Liu, Jiacheng Guo, Yuan Du**
7307	1	**Title:** A 13–18 GHz Low-Power Multi-Modulus Frequency Divider in 55-nm CMOS **Author:** **Junhao Huo, Yuzhou Li, Dixian Zhao**

LECTURE SESSION - DAY 2

Time: **16:00-17:30**
Date: **October 22, 2025, Thursday**

Session - SS15.17: Next-Generation Wireless Technologies for Biomedical and IoT Applications

Session Chair: **Hyun-su Lee**

Session code: **B5L-A**		
Venue: **Lecture 1 - Waterfront Ballroom 1**		
Paper ID	**Track**	**Paper Info.**
7355	15.17	**Title:** Advances in Multi-Output Wireless Power Regulators with a Single Coil **Author:** **Hyun-Su Lee**
7356	15.17	**Title:** Advances in Multi-Output Wireless Adiabatic Stimulators with a Single Coil **Author:** **Hyun-Su Lee**
7179	15.17	**Title:** A Low-Power Scalable Multicarrier Generator Using Current-Domain Waveform Replication **Author:** **Hoang Son Thai, Shenshaoju Chen, Tong Ge**
7246	15.17	***INVITED*** **Title:** Beyond Fixed Supply: Average Power Tracking, Envelope Tracking, and Symbol Power Tracking for Energy-Efficient Wireless Transmitters **Author:** **Shenshaoju Chen, Tong Ge**
7076	15.17	**Title:** A Low Power IR-UWB Detector to Baseband Chain with Self-Mixing Energy Detection and Tunable Baseband Gain **Author:** **Mohan Li, Xuan Zhang, Lei Yao**
7296	15.20	**Title:** Circuit Co-Design of Air-Coupled Ultrasond Imaging System for UAV Applications **Author:** **Jiaqi Guo**

LECTURE SESSION - DAY 2

Time: **16:00-17:30**
Date: **October 22, 2025, Thursday**

Session - SS15.19: Compute-in-memory architectures, circuits and devices for next-generation AI systems

Session Chair: **Yuqi Su**

Session code: **B5L-B**		
Venue: **Lecture 2 - Waterfront Ballroom 2**		
Paper ID	**Track**	**Paper Info.**
7101	15.19	**Title:** A 6.78-MHz 20-W 96.2%-Peak-Efficiency Single-Stage Wireless Power Receiver with an Efficient Driver-Supply Generating Technique **Author: Junfei Ge, Dongfang Pan, Lin Cheng**
7194	15.19	**Title:** A Scalable Multi-Input Piezoelectric Array Energy Harvesting Circuit with Arbitrary Phase Offset and Flying Capacitor Sharing **Author: Yikun Liu, Shousheng Han, Yuhui Shu, Yuhan Wang, Dan Xie, Xiaoming Wu, Xiaosen Liu, Yan Lu, Tian-Ling Ren**
7254	15.19	**Title:** A Fully Integrated Phase-Interleaved High-Density Inverting Charge Pump for Wearable LCD Display **Author: Wei Li, Chen Hu, Tiantian Tang, Xingyuan Li, Pishu Liang, Tianping Sun, Jianchao Xu, Junmin Jiang**
7275	15.19	**Title:** A Half-Bridge GaN Driver with On-Chip CISS-Variation Sensing for Device Health Monitoring **Author: Xiaoyu Wang, Hangxiao Ma, Qiaobo Ma, Yang Jiang, Rui P. Martins, Pui-In Mak**
7308	15.19	**Title:** A Power-to-Voltage Converter-Based MPPT Boost Converter for Micro Energy Harvesting **Author: Youlin Wu, Chenchang Zhan**
7330	15.19	**Title:** A Configurable Continuous-Time Integrator for a Reconfigurable Analog Computing Chip **Author: Sara Obergassel, Pavol Pitonak, Dirk Killat, Bernd Ulmann, Johannes Fritzsche**

LECTURE SESSION - DAY 2

Time: **16:00-17:30**
Date: **October 22, 2025, Thursday**

Session - SS15.16: Domain-specific Hardware Design for Perception of UAVs, Humanoid Robots and Autonomous Vehicles

Session Chair: **Ye Liu**

Session code: **B5L-C**		
Venue: **Lecture 3 - Waterfront Ballroom 3**		
Paper ID	**Track**	**Paper Info.**
7273	15.16	***INVITED*** **Title:** An FPGA-Based EKF Accelerator with an Efficient Matrix Solver for Visual SLAM **Author: Dian Yuan, Ke Yang, Chenlin Zhou, Yunxin Cui, Xiuyuan Qi, Chaoyue Chen, Jun Zhou, Ye Liu**
7247	15.16	**Title:** An Energy-Efficient Reconfigurable NoC-Based YOLO Hardware Accelerator with Workload Balancing and Pre-Loading Zero-Skipping for Edge Vision Applications **Author: Ziang Duan, Zixuan Shen, Jiajun Wu, Yuansheng Zhao, Zhigang Wu, Peng Zhou, Jiang Tang, Chao Wang**
7212	15.16	**Title:** THOR-SR: A Computation-Efficient Tile-Halo Optimized FPGA Accelerator for RFDN-Based Image Super-Resolution **Author: Yi Wang, Lujie Peng**
7160	15.16	**Title:** An Efficient LiDAR Odometry Accelerator with Compact Feature Transfer and Adaptive Search **Author: Zhao Cang, Yaotang Wu, Yongming Tang, Hao Sun**
7139	15.16	**Title:** A Lightweight Task-Calibrated Screening Framework with Closed-Loop Latency Prediction for Early-Stage RISC-V UAV Processing System Design **Author: Yifei Cheng, Yujie Ma, Chixiao Chen, Haozhe Zhu**
7121	15.16	**Title:** An RRAM CIM Phase Correlation Accelerator with Reliability Gated Phase Indexing for UAV Image Registration **Author: Jiaqi Yu, Shulin Zhu, Liang Zhao**

LECTURE SESSION - DAY 3

Time: **08:30-10:00**
Date: **October 23, 2025, Friday**

Session - In-memory Computing Devices

Session Chair: **Lin Bao, Zongwei Wang**

Session code: **C1L-A**		
Venue: **Lecture 1 - Waterfront Ballroom 1**		
Paper ID	**Track**	**Paper Info.**
7112	9	**Title:** Image Encryption via Temporal Plasticity in Ga_2O_3 Optoelectronic Synapses **Author: Mengyue Yue, Cizhe Fang, Yibo Wang, Bing Chen, Yan Liu, Yue Hao, Genquan Han**
7172	9	**Title:** A 1T1R Array Integrating Weight-Independent Physical Unclonable Function and Flexible In-Memory Computing **Author: Borui Shi, Houcheng Liu, Zongwei Wang, Yimao Cai**
7183	9	**Title:** A Novel Voltage-Differential True Random Number Generator with Near-Full Entropy **Author: Tianci Wang, Xibo Chen, Xinshuai Gao, Xiao Yu, Xiguang Wu, Bing Chen, Yan Liu, Genquan Han**
7227	9	**Title:** Ar^+ Ion Implantation Engineered Stochasticity in Self-Rectifying Memristors for Concealable and Reconfigurable PUFs **Author: Yunhui Yi, Puyi Zhang, Yibai Xue, Jiancong Li, Zirui Li, Wenbin Zuo, Yi Li, Xiangshui Miao**
7252	9	**Title:** An Energy-Efficient and High-Accuracy Position-Encoded RRAM Aging Monitor for Reliable Compute-in-Memory Systems **Author: Zixuan Shen, Sunbin Deng, Yingchen Ji, Jiarui Xu, Haoran Wang, Zhanlong Lou, Yimao Cai, Zongwei Wang, Chao Wang**
7286	9	**Title:** Attention-in-Memory: Neural Turing Machine Based on NOR-Type FeFET Array for Algorithmic Inference **Author: Zhibin Qian, Liying Peng, Yihao Zang, Depu Zhao, Qingdong Yu, Jun Li, Jie Yu, Zhongguang Xu**

LECTURE SESSION - DAY 3

Time: **08:30-10:00**
Date: **October 23, 2025, Friday**

Session - Design Automation and Optimization

Session Chair: **Prof. Jing Tian**

Session code: **C1L-B**		
Venue: **Lecture 2 - Waterfront Ballroom 2**		
Paper ID	**Track**	**Paper Info.**
-	-	* INVITED * **Title:** AI-driven RF Circuits for Handset Applications **Author:** **Xinyu Zhou**
7074	8	**Title:** Evidence-Driven PDK-IP Co-Readiness Assessment and Regression Routing Under Automotive Constraints **Author:** **Kumaran Sundaram**
7279	8	**Title:** PPO-Based Reinforcement Learning for Automated Distributed Matching Network Synthesis in RF Energy Harvesting Systems **Author:** **Ritoo Verma, Gurumurthy Hegde, Pratyay Dutta, Laxmeesha Somappa, Maryam Shojaei Baghini**
7203	8	**Title:** Adaptive Threshold Refinement for CPWL Digital Predistortion **Author:** **Dandan Teng, Qing Luo, Xiaowei Zhu, Peng Chen, Chao Yu**
7028	8	**Title:** Efficient High-Speed Link Optimization via Transfer-Learning-Assisted High-Fidelity Bayesian Optimization **Author:** **Xiao-Yang Wu, Da-Wei Wang, Wen-Sheng Zhao**
7319	8	**Title:** Tier-Wise Recovery and Simulator-Audited Reasoning in an Un-Augmented LLM Analog Design Loop **Author:** **Moustafa Nawito**

LECTURE SESSION - DAY 3

Time: **08:30-10:00**
Date: **October 23, 2025, Friday**

Session - SS15.9: Evolving RF, mm-Wave, and THz Front-Ends for Next-Generation Sensing and Communication Systems

Session Chair: **Xiang Yi**

Session code: **C1L-C**		
Venue: **Lecture 3 - Waterfront Ballroom 3**		
Paper ID	**Track**	**Paper Info.**
7343	15.9	**Title:** New Progresses in CMOS Oscillators **Author:** **Pei Qin**
7346	15.9	***INVITED*** **Title:** Reconfigurable RF Front-End Amplifiers for Multi-Band Communication Applications (Invited Talk) **Author:** **Haoshen Zhu**
7144	15.9	***INVITED*** **Title:** 300-GHz 2D CMOS Phased-Array Transmitter and Receiver with Near-Half-Wavelength Antenna Pitch for Communication Applications (Invited Talk) **Author:** **Kaizhe Guo**
7106	15.9	**Title:** Wideband GaN Front-End and Variable-Gain Amplifier **Author:** **Cao Wan, Zhuowei Xie**
7047	15.9	***INVITED*** **Title:** Dual-Band FMCW Radar Transceiver: From Sparse Synthetic Bandwidth Radar Concept to Sub-mm 3D Imaging (Invited Talk) **Author:** **Xiang Yi**
7008	15.9	**Title:** A 1.3-4.8 GHz Reconfigurable Low-Pass Filter Using Dual Capacitor Tuning Techniques in 0.15-µm GaAs **Author:** **Yijie Zhang, Jiang Wang, Hao Ning, Zhaowu Wang, Shuo Li, Yixin Hu, Xiaochen Tang, Yong Wang**

LECTURE SESSION - DAY 3

Time: **10:10-11:40**
Date: **October 23, 2025, Friday**

Session - Efficient Accelerators for AI and Cryptography

Session Chair: **Ye Liu, Chao Wang**

Session code: **C2L-A**		
Venue: **Lecture 1 - Waterfront Ballroom 1**		
Paper ID	**Track**	**Paper Info.**
7237	4	**Title:** RASC: Runtime Channel-Aware Mixed Precision and Shared-Recode FP Computing for Low-Bit VAR Inference **Author:** **Bo Hu, Xinyang Chen, Jiaming Lin, Shun Zhang, Peng Zheng, Yu Gong, Hao Cai, Bo Liu**
7038	4	**Title:** MGFA: A Modality-Aware Glance-and-Focus Accelerator for High-Resolution VLM Inference **Author:** **Han Zhang, Xinxin Zhang, Haolin Ge, Xingyi Wang, Kaiying Yang, Jing Cao, Xiaoyan Hu, Fengbin Tu, Biao Pan**
7309	4	**Title:** A Hardware-Software Co-Design of Dynamic Activation Quantization for Edge Vision-Language-Action Models **Author:** **Haolong Li, Jin Wang, Xun Zhang, Longyang Lin**
7187	4	**Title:** A Doppler-Track Fusion CNN Accelerator for Low-Altitude Radar Target Classification **Author:** **Weixuan Wang, Bo Wang, Dixian Zhao**
7282	4	**Title:** Low-Overhead Address Mapped NTT Domain Automorphism Design for CKKS Accelerators **Author:** **Pengfei Sun, Makoto Ikeda**
7294	4	**Title:** A Lightweight Fused Floating-Point & Modular Arithmetic Unit for FALCON FFT/NTT **Author:** **Mingbo Wang, Tianze Huang, Yibo Wang, Dongsheng Liu, Jiahao Lu**

Session - Domain Specific and AI Assisted ICs

Session Chair: **Lujie Peng, Tao Tang**

Session code: **C2L-B**		
Venue: **Lecture 2 - Waterfront Ballroom 2**		
Paper ID	**Track**	**Paper Info.**
7263	13	**Title:** A Lightweight Hardware Architecture for Secure Federated Learning **Author:** **Jiaqi Tang, Yue Zheng, Michael Kwok-Po Ng, Chip Hong Chang, Yongkui Yang**
7317	13	**Title:** A 35.88 μW MVFE-Gait Processor for Piezoelectric Power-Based Gait Recognition **Author:** **Zihao Chen, Ziang Wang, Zhenghao Li, Jiamin Li**
7336	13	**Title:** A 40nm 16.6 mat/μJ Outer-Product-Based SVD Processor with Matrix Element Position Aligned PEs and Parallel Jacobi Method **Author:** **Dongrui Li, Mohamed Mukhtar, Anh Tuan Do, Bo Wang**

LECTURE SESSION - DAY 3

Time: **10:10-11:40**
Date: **October 23, 2025, Friday**

Session - Domain Specific and AI Assisted ICs

Session Chair: **Lujie Peng, Tao Tang**

Session code: **C2L-B**		
Venue: **Lecture 2 - Waterfront Ballroom 2**		
Paper ID	**Track**	**Paper Info.**
7078	13	**Title:** Embedding Circuit Knowledge Into Surrogates: Physics-Informed Bayesian Optimization of a Class-C LC VCO in 40-nm CMOS **Author: Huynh Nguyen Toan Thang, Jithish Jayarajan, Nagarajan Mahalingam, Songnan Yang, Haoyang Liu, Kiat Seng Yeo**
7238	13	**Title:** RFEC: A Padding-Free Rotation and Factorized Encoded-Computing Accelerator for FP4 VARs **Author: Xinyang Chen, Jiaming Lin, Bo Hu, Shun Zhang, Peng Zheng, Puyang Hong, Yu Gong, Hao Cai, Bo Liu**
7052	13	**Title:** A Tanh-First Multiplier-Free Shared Sigmoid and Tanh Activation Circuit with Micro-Residual Compensation **Presenter: Chaohong Zhang, Yida Chen, You Du, Xueyong Zhang, Shen Xu, Weifeng Sun**

Session - High-Speed Wireline and Optical Circuits

Session Chair: **Xin Wang, Fuzhan Chen**

Session code: **C2L-C**		
Venue: **Lecture 3 - Waterfront Ballroom 3**		
Paper ID	**Track**	**Paper Info.**
7362	5	**Title:** Co-Design of Electronic and Photonic Integrated Circuits for High-BW DWDM Transceivers (Invited Talk) **Author: Nan Qi**
7331	5	**Title:** A 200 GBaud Broadband Amplifier in 28nm CMOS **Author: Chen Zhang, Xiaoqi Peng, Mengqi Wu, Bowen Zhang, Zhen Chen, Junbo Zhu, Peng Li, Chu Tang, Daoqun Liu, Yutao Tang, Yu Zheng, Lei Wang, Ke Li**
7348	5	**Title:** A 4× 25.2-Gb/s/Wire Data and Clock Simultaneous Bidirectional Transceiver in 65-nm CMOS for Active Interposer **Author: Yuhao Zhang, Xiaoteng Zhao, Qi Zhang, Zhanming Gao, Chenxi Han, Zhicheng Dong, Jie Wang, Hongzhi Liang, Lin Wang, Zhou Shu, Shubin Liu, Zhangming Zhu**
7040	5	**Title:** A 12.8–15.2 GHz CPPLL Employing a Supply-Pushing Reduction VCO with >57% Frequency-Variation Suppression **Author: Yiheng Hui, Yuanlin Nong, Jinpeng Zhu, Qian Liu, He Ma, Jingjing Lv, Dawei Li, Li Du, Yuan Du**

LECTURE SESSION - DAY 3

Time: **10:10-11:40**
Date: **October 23, 2025, Friday**

Session - High-Speed Wireline and Optical Circuits

Session Chair: **Xin Wang, Fuzhan Chen**

Session code: **C2L-C**		
Venue: **Lecture 3 - Waterfront Ballroom 3**		
Paper ID	**Track**	**Paper Info.**
7244	5	**Title:** A 56-Gb/s 0.295-pJ/Bit Two-Stage Inverter-Based CTLE Front-End with Programmable Peaking and Group-Delay Control in 22-nm CMOS **Author:** **Zian Deng, Yuhao Yang, Yuyang Luo, Liheng Lou, Robert Bogdan Staszewski, Yizhe Hu**
7059	5	**Title:** A 13.27–14.67 GHz Class-F23 VCO with Temperature-Drift Compensation Circuit Achieving a Frequency Temperature Coefficient of 2.86 ppm/°C in 28 nm CMOS **Author:** **Jinpeng Zhu, Yiheng Hui, Yuanlin Nong, Qian Liu, Dawei Li, Jingjing Lv, Li Du, Yuan Du**

Time: **12:30-14:00**
Date: **October 23, 2025, Friday**

Session - SS15.12: Advanced CMOS RF and mmWave Frond-end Circuits

Session Chair: **Fanyi Meng**

Session code: **C4L-A**		
Venue: **Lecture 1 - Waterfront Ballroom 1**		
Paper ID	**Track**	**Paper Info.**
7006	15.12	**Title:** A 16-to-32.5 GHz Dual-Core Quad-Mode VCO **Author:** **Kaiqiang Qin, Huynh Nguyen Toan Thang, Nagarajan Mahalingam, Bharatha Kumar Thangarasu, Xiang Maoyang, Fanyi Meng, Kaixue Ma, Kiat Seng Yeo**
7233	15.12	***INVITED*** **Title:** VCO Pulling in Low Phase Noise VCO for RADAR Applications **Author:** **Anqing Chen, Hai Ye, Nagarajan Mahalingam, Bharatha Kumar Thangarasu, Fanyi Meng, Kaixue Ma, Kiat Seng Yeo**
7235	15.12	**Title:** A 25.6 to 47.3 GHz Broadband Power Amplifier with 18.1 dBm P_{sat} and 32.2% PAE in 40-nm CMOS **Author:** **Zhenyu Zhang, Hongshi Yu, Bharatha Kumar Thangarasu, Nagarajan Mahalingam, Fanyi Meng, Kaixue Ma, Kiat Seng Yeo**
7240	15.12	**Title:** A 1 V, 3.3 mW Low-Noise Amplifier for 2.4 GHz IoT Receivers with 18.4 dB Gain, 2.3 dB NF and Enhanced Linearity **Author:** **Xinyu Wang, Hai Ye, Bharatha Kumar Thangarasu, Nagarajan Mahalingam, Fanyi Meng, Kaixue Ma, Kiat Seng Yeo**

LECTURE SESSION - DAY 3

Time: **12:30-14:00**
Date: **October 23, 2025, Friday**

Session - SS15.12: Advanced CMOS RF and mmWave Frond-end Circuits

Session Chair: **Fanyi Meng**

Session code: **C4L-A**		
Venue: **Lecture 1 - Waterfront Ballroom 1**		
Paper ID	**Track**	**Paper Info.**
7249	15.12	**Title:** Design of a High Gain Low Noise Amplifier in 40 nm CMOS Process for IoT Applications **Author:** **Shuoyu Ji, Yuqing Liu, Bharatha Kumar Thangarasu, Nagarajan Mahalingam, Jithish Jayarajan, Baoji Miao, Fanyi Meng, Kaixue Ma, Kiat Seng Yeo**
7256	15.12	**Title:** A 17–33 GHz 40 nm CMOS LNA with 21.5 dB Peak Gain and 2.52 dB Minimum NF for K/Ka Band Receivers **Author:** **Yue Tian, Sini Wu, Bharatha Kumar Thangarasu, Nagarajan Mahalingam, Fanyi Meng, Kaixue Ma, Kiat Seng Yeo**

Session - SS15.4: IC based modules, system integration and applications

Session Chair: **Hu Fang**

Session code: **C4L-B**		
Venue: **Lecture 2 - Waterfront Ballroom 2**		
Paper ID	**Track**	**Paper Info.**
7315	15.4	**Title:** A Portable Standalone FPGA-Based Microfluidic Impedance-Activated Particle Sorting Platform with Real-Time Signal Processing **Author:** **Zhe Tang, Jin Chen, Xiwei Huang, Lingling Sun, Chiang Liang Kok, Jovan Heng Bowen, Tee Hui Teo**
7117	15.4	**Title:** Wavelet-SCORE: A Community Detection Algorithm for Integrated-Circuit Connectivity Networks **Author:** **Yanhui Zhu, Jia Liu, Christian Addotta, Connor Birkland**
7069	15.4	**Title:** AWA-CML: An Adaptive Weighted Attention-Enhanced Cross-Modal Learning Framework for Intelligent Diagnosis **Author:** **Wenwen Yue, Qun Li, Lina Wu, Fang Hu**
7057	15.4	***INVITED*** **Title:** SM-MDFL: Semantic-Matching Multimodal Decoupled Feature Learning Framework for Zero-Shot Image Recognition **Author:** **Chaolei Wu, Ziyi Deng, Fang Hu, Yin Zhang**
7035	15.4	**Title:** Authenticated and Efficient Join Query for Multi-Blockchain Medical Systems **Author:** **Jian Chang, Kun Li, Xiaoling Zhou**
7075	15.4	**Title:** HOS-HGL: A High-Order Similarity-Guided Hybrid Graph Learning Framework for Prescription Recommendation **Author:** **Caidie Li, Mengyuan Jin, Meng Zhang**

LECTURE SESSION - DAY 3

Time: **12:30-14:00**
Date: **October 23, 2025, Friday**

Session - SS15.8: Energy-Efficient Circuits and Systems for Intelligent Sensing and Wireless Data/Energy transfer

Session Chair: **Atila Alvandpour**

Session code: **C4L-C**		
Venue: **Lecture 3 - Waterfront Ballroom 3**		
Paper ID	**Track**	**Paper Info.**
7015	15.8	**Title:** Thermal-Noise-Driven Design of an Amplifier-Less Continuous-Time ADC **Author: Hampus Malmberg, Baktash Behmanesh, Alireza Saberkari**
7020	15.8	**Title:** A 32-Input Mixed-Signal WTA Router for CIM-Based MoE Top-k Selection **Author: Haoran Yi, Alireza Saberkari, Atila Alvandpour**
7021	15.8	**Title:** Injectable Wireless Soft Bioelectronic On-Chip Platform for Programmable Neural Stimulation **Author: Natachai Terawatsakul, Venkata Kishore Perla, Jakob von Heideken, Aiman Rahmanudin, Klas Tybrandt, Alireza Saberkari**
7024	15.8	*** INVITED *** **Title:** Dual-Mode Cavity and ASIC Co-Design Solution for Simultaneous WPT and Backcom in Miniaturized Implants **Author: Alireza Saberkari**
7114	15.8	**Title:** A 13.56-MHz Hybrid-Compensated CMOS Rectifier for Low-Power Wireless Power Transfer **Author: Wei Cao, Natachai Terawatsakul, Alireza Saberkari, Atila Alvandpour**
7191	15.20	**Title:** A Low-Power Wearable Sign Language Recognition System Based on Multimodal Fusion with a BiLSTM Network **Author: Lulu Huang, Weiwei Shi, Siyi Li**

LECTURE SESSION - DAY 3

Time: **14:05-15:20**
Date: **October 23, 2025, Friday**

Session - Emerging Semiconductor Devices

Session Chair: **Sunbin Deng**

Session code: **C5L-A**		
Venue: **Lecture 1 - Waterfront Ballroom 1**		
Paper ID	**Track**	**Paper Info.**
7022	9	**Title:** Thin-Barrier AlGaN/GaN MISHEMTs on Si Achieving 2.81 W/mm Power Density at Vds = 9 V for Millimeter-Wave Mobile Terminal Applications **Author:** **Mengdi Li, Jiejie Zhu, Yifan Chen, Wanshuo Liao, Fei Wu, Yue Hao, Xiaohua Ma**
7062	9	**Title:** Dynamic Wafer-to-Wafer Uniformity Control in PVD Using Real-Time Plasma Mapping **Author:** **Ravi Kiran Boyidi, Sim Kit Wang**
7110	9	**Title:** Reliability Enhancement in $Hf_{0.5}Zr_{0.5}O_2$ Capacitors via Oxygen Annealing Surface Modification **Author:** **Xiaolong Jing, Zichong Zhang, Wenxi Zhou, Rui Su, Xiangshui Miao, Xingsheng Wang**
7143	9	**Title:** Heterogeneously Integrated GaN/SiC Cascode HyFETs for 800-V AI Server Power Supplies **Author:** **Xiaoming Ge, Sichao Li, Yimo Li, Tao Cheng, Shuangzan Lu, Jiajun Han, Zhikun Tao, Yu Zhai, Jieqiong Zhang, Jun Liu, Hongye Yang, Ruolan Wang, Liping Yin**
7155	15.21	**Title:** A 0.0038-mm² CMOS Temperature Sensor with Direct Offset-to-Digital Conversion Based on a Sensing-Embedded Delta-Sigma Modulator **Author:** **Yichi Zhang, Chenfeng Wang, Aili Wang**

Session - Analog Circuit Techniques

Session Chair: **Yuan Gao, Yuxuan Luo**

Session code: **C5L-B**		
Venue: **Lecture 2 - Waterfront Ballroom 2**		
Paper ID	**Track**	**Paper Info.**
7142	2	**Title:** A High-Accuracy BiCMOS All-in-One Bandgap Voltage and Current Reference Without Amplifiers **Author:** **Chengcheng Liu, Chen Deng, Yixuan Miao, Yatao Peng, Jun Yin, Rui P. Martins, Pui-In Mak**
7176	2	**Title:** A 0.3–0.6 V, 25.6 MHz–1.94 GHz Dual-Path SPD/PFD Ultra-Low-Voltage PLL **Author:** **Chengyu Yang, Zirui Jin, Jingsong Cui**
7241	2	**Title:** A 2.49V-to-11.85V 0.13V-per-Step Fine-Coarse Tuning Bias Circuits for MEMS Microphones **Author:** **Hung-Ting Han, Qi Zhang, Jiaqi Dong, Zipeng Cheng, Zuyang Cao, Xin Zhang, Bo Zhao, Yuxuan Luo**

LECTURE SESSION - DAY 3

Time: **14:05-15:20**
Date: **October 23, 2025, Friday**

Session - Analog Circuit Techniques

Session Chair: **Yuan Gao, Yuxuan Luo**

Session code: **C5L-B**		
Venue: **Lecture 2 - Waterfront Ballroom 2**		
Paper ID	**Track**	**Paper Info.**
7305	2	**Title:** A Programmable Analog Baseband Circuit for FMCW Millimeter-Wave Radar in 55-nm CMOS **Author: Yunpeng Cui, Dixian Zhao**
7312	2	**Title:** A 145 Gb/s TIA with Inductor-Enabled Noise Suppression Demonstrating Pam-6 Operation in SiGe BiCMOS **Author: Zhihan Zhang, Bolun Cui, Ruogu Deng, Jingbo Wang, Ruihan You, Guike Li, Nan Qi, Liyuan Liu, Lei Wang**

Session - SS15.14: Millimeter-Wave and Terahertz Signal Generation for Next-Generation Communications and Sensing

Session Chair: **Yuan Gao, Yuxuan Luo**

Session code: **C5L-C**		
Venue: **Lecture 3 - Waterfront Ballroom 3**		
Paper ID	**Track**	**Paper Info.**
7341	15.14	***INVITED*** **Title:** Design of Low-Voltage Low-Jitter Fractional-N PLL: An Overview (Invited Talk) **Author: Zhao Zhang**
7136	15.14	***INVITED*** **Title:** An LC-Based Multi-PLL System for Flexible Clocking in Wireline Transceivers **Author: Chuqiao Wang, Dingshuo Liu, Xia Jing, Danfeng Xu, Haoyuan Gao, Jianzhe Feng, Xiaolong Liu**
7087	15.14	**Title:** A 90–96-GHz Frequency Synthesizer with a Harmonic-Mixing-Based Frequency Quintupler in 65nm CMOS **Author: Kaitian Yang, Shuo Tian, Longyang Lin, Xiaolong Liu**
7048	15.14	**Title:** A 1.05-to-7.35-GHz Ring-Based Fractional-N ADPLL in 12nm FinFET **Author: Shuo Tian, Chuqiao Wang, Weiming Wang, Weirong Yao, Xia Jing, Xiaolong Liu**
7200	15.22	**Title:** A 12-Bit Area-Efficient SAR ADC with Digital Calibration for HgCdTe Infrared Focal-Plane Array Readout **Author: Yixuan Lu, Dejian Li, Jiali Hou, Mengqian Jiang, Siyuan Ma, Liguo Liu, Peiyuan Wan, Zhijie Chen**

LECTURE SESSION - DAY 3

Time: **15:25-16:55**
Date: **October 23, 2025, Friday**

Session - SS15.18: Advanced Power Delivery for AI Computing: System Architectures, Modeling, and Converter Innovations

Session Chair: **Zhiguo Tong**

Session code: **C6L-A**		
Venue: **Lecture 1 - Waterfront Ballroom 1**		
Paper ID	**Track**	**Paper Info.**
7123	15.18	**Title:** A 4-V Input 0.5–1.5-V Output CSCR-Middle Hybrid Switched-Capacitor Converter for XPU PoL Regulation **Author:** **Du Zhou, Mo Huang, Guigang Cai**
7138	15.18	**Title:** Chiplets PDN Modeling Framework with Decomposed Perturbation in SSA Based on LEGO-VRM **Author:** **Hongda Yu, Wen-Liang Zeng, Ping Wang, Cheng Gong, Wenning Jiang, Chi-Seng Lam**
7226	15.18	**Title:** Ai Next-Gen Power Delivery: Vcore Evolution & Future Trends **Author:** **Danzhu Lyu**
7271	15.18	**Title:** A 36-A Fully Analog Distributed LDO with Single-Line Voltage-Margin-Adaptive Current Sharing **Author:** **Naiqi Wang, Yan Lu**
7278	15.18	***INVITED*** **Title:** PWM Aliasing Effects of Current-Sharing Loops in Multiphase Buck Converters **Author:** **Ziyao Dang, Yan Lu, Zhiguo Tong**
7014	3	**Title:** An LDO Design Methodology Using Staged Multi-Objective Bayesian Optimization with Learned Feasibility Discovery **Author:** **Sini Wu, Jithish Jayarajan, Bharatha Kumar Thangarasu, Nagarajan Mahalingam, Kiat Seng Yeo**

LECTURE SESSION - DAY 3

Time: **15:25-16:55**
Date: **October 23, 2025, Friday**

Session - SS15.20: Innovative Circuits and Systems: From Sensing to Intelligent Computing

Session Chair: **Jerald Yoo**

Session code: **C6L-C**		
Venue: **Lecture 3 - Waterfront Ballroom 3**		
Paper ID	**Track**	**Paper Info.**
7303	15.20	***INVITED*** **Title:** Design and Analysis of Energy- and Area-Efficient Sensor Interface Circuits **Author: Jerald Yoo**
7301	15.20	**Title:** LUNARCH: AI-Driven Chip Design Leveraging Open-Source Toolchains **Author: Han Wu**
7299	15.20	**Title:** A Reconfigurable CMOS Ising Machine with Self-Adaptive Energy Feedback Annealing **Author: Yingna Huang, Chne-Wuen Tsai, Zhongqi Li, Jiaer Chen, Jerald Yoo**
7298	15.20	**Title:** Hybrid Time- /Voltage-Domain Residue Amplification: Enabling High-Speed High-Resolution Pipelined SAR ADCs **Author: Rucheng Jiang, Zhe Liu**
7297	15.20	**Title:** An Efficient Ultrasound-Powered Bio-Stimulator with Real-Time Communication and Precise Regulation **Author: Jiamin Li**
7285	15.20	**Title:** Breaking the Barriers of Neural Interfacing: From High-Fidelity Wearables to Ultra-Compact Implants **Author: Tao Tang**

POSTER SESSION - DAY 1

Time: **11:50-13:15**
Date: **October 21, 2025, Wednesday**
Venue: **Foyer**

Session - RF Circuits

Session Chair: **Loo Xi Sung**

Session code: **A2P-D**			
No.	**Paper ID**	**Track**	**Paper Info.**
P01	7132	1	**Title:** A 15.98–19.02 GHz 65 nm CMOS Wide-Tuning-Range LC-VCO with Enhanced Tuning Linearity Based on Differential Complementary Varactor Arrays **Author:** **Haoran Jiang, Zongming Duan, Zhipeng Wang**
	7272	1	**Title:** 4–8-GHz Quad-Band Cryogenic SiGe LNA with 4-to-1 Current Combining for FDM Qubit Readout **Author:** **Yixuan Miao, Zhuo Xu, Fengen Yuan, Chengcheng Liu, Yatao Peng, Jun Yin, Rui P. Martins, Pui-In Mak**

Session - Processor and Chiplet Architectures

Session Chair: **Fengbin Tu, Xin Si**

Session code: **A2P-E**			
No.	**Paper ID**	**Track**	**Paper Info.**
P02	7154	4	**Title:** Multi-Directional Shift-Based Self-Repair for Chiplet Interconnects with Clustered Fault **Author:** **Xiaowen Jiang, Pengkang Luo, Guowei Xing, Qimin Yuan, Kai Huang**
	7209	4	**Title:** A RISC-V Based Vector Processor with Hardware–Software Co-Design of Softmax and LayerNorm Accelerator **Author:** **Siyu Cao, Haoran Geng, Cheng Liu, Li Du**

Session - High-Speed Wireline and Optical Circuits (poster)

Session Chair: **Fuzhan Chen, Xin Wang**

Session code: **A2P-F**			
No.	**Paper ID**	**Track**	**Paper Info.**
P03	7025	5	**Title:** A 256-Gbps 4-Vppd Distributed Modulator Driver with 3-Ps Group Delay Variation in 22-nm Bulk CMOS **Author:** **Ruixuan Yang, Yifei Xia, Yuye Yang, Jianyu Yang, Li Geng, Dan Li**
	7333	5	**Title:** A 20-40 GHz Quadruple-Mode VCO with Reconfigurable E-M Hybrid-Coupling for Reference-Less CDR in 28-nm CMOS **Author:** **Xuanyu Li, Pingyi Cai, Wenhan Guan, Hongzhi Wu, Quan Pan**

POSTER SESSION - DAY 1

Time: **11:50-13:15**
Date: **October 21, 2025, Wednesday**
Venue: **Foyer**

Session - Chips and Systems for Intelligent Robot

Session Chair: **Zhuo Zou, Mingyu Wang**

Session code: **A2P-H**			
No.	**Paper ID**	**Track**	**Paper Info.**
P05	7140	12	**Title:** A 134.90-kedges/s Real-Time FPGA Accelerator for Collision Checking in Robot Motion Planning **Author:** **Linqi Li, Yujie Ma, Sinong Gong, Chixiao Chen, Haozhe Zhu**
	7290	12	**Title:** sEMG-Based Gesture Recognition Using Spiking Neural Network with Bipolar Activations and Quantized Weights **Author:** **Baixiang Wu, Shuo Yuan, Xiangyu Xu, Zhixing Hou, Xiao Wang, Ziming Chen, Tianlin Liang, Rangyu Deng, Chio-In Ieong**

Session - AI for ICs

Session Chair: **Fengbin Tu, Xin Si, Do Anh Tuan**

Session Code: **A2P-I**			
No.	**Paper ID**	**Track**	**Paper Info.**
P06	7222	13	**Title:** FPGA-Aware Position-Aligned SNN for OFDR Phase-Error Estimation **Author:** **Qianyi Li, Yujie He, Dong Jiang, Enyi Yao**
	7253	13	**Title:** CuPulseForge: An Evidence-Gated GPU Front End for Multidomain Radio Frequency Classification **Author:** **Yichen Ding, Yunchang Jiang, Dong Jiang, Zhanhong Huang, Enyi Yao**
	7267	13	**Title:** Multi-Fidelity Pareto-Aware Bayesian Optimization for RF Multiplexer Design **Author:** **Siyuan He, Zhun Wei**

Session - Micro-nano Optoelectronic Chips and Integrated Devices 1

Session Chair: **Weicong Na, Baolu Guan**

Session code: **A2P-J**			
No.	**Paper ID**	**Track**	**Paper Info.**
P07	7043	15	***INVITED*** **Title:** Neural Space Mapping Based Multiphysics Inverse Modeling for Microwave Filter Design **Author:** **Weicong Na, Siyao Yu, Feng Feng, Xu Liu, Baolu Guan**
	7206	15	**Title:** A 128×128 Four-Column-Shared Column-Parallel CMOS ROIC with a Second-Order Fully Passive Noise-Shaping SAR ADC for Cooled MWIR Focal-Plane Arrays **Author:** **Mengqian Jiang, Hongyou Li, Dezhen Yang, Yuxuan Peng, Peiyuan Wan, Xu Liu, Zhijie Chen**

POSTER SESSION - DAY 2

Time: **11:50-13:15**
Date: **October 22, 2025, Thursday**
Venue: **Foyer**

Session - Analog Techniques and Power Management

Session Chair: **Yuan Gao, Yang Jiang**

Session code: **B2P-D**			
No.	**Paper ID**	**Track**	**Paper Info.**
P01	7011	2	**Title:** A Dual-Frequency 26MHz/1MHz Clock Generator with Anti-Glitch Switching in 14nm FinFET for UFS Controller SoCs **Author:** **Qun Li, Chi-Hang Chan, Bin Liu, Pui-In Mak, Rui P. Martins, Nai Lai, Ka-Meng Lei**
	7281	2	**Title:** A 180-nm CMOS 1024× Ring-Amplifier Residue Amplifier with Replica-Biased PVT Stabilization and Correlated Level Shifting **Author:** **Zijian Li, Zelong Chen, Kaile Qin, Mingyu Lai, Lei Zhang**
	7245	3	**Title:** A 7.5 μA Quiescent Current, 4 - 60 V Input Voltage Range LDO Regulator with 96X Adjustable Output Voltage Range for Industrial and Automotive Electronic Applications **Author:** **Zhen Wang, Shiquan Fan, Wenhan Sun, Ruiqi Song, Boyu Luo, Feng Liang, Guohe Zhang**
	7324	3	**Title:** Switching Loss Optimization of Multi-Stacked Switched Capacitor Converters **Author:** **Haoqiang Deng, Zhendong Li, Yifan Jiang, Bowen Zheng, Peidong Zeng, Xi Luo, Chen Hu, Xun Liu, Junmin Jiang**
	-	-	***INVITED*** **Title:** A Direct Drive Solution for D-Mode GaN HEMT with Integrated Current Monitoring for AI Data Center Power Supplies **Author:** **Xuetong Zhou**

Session - Biomedical ICs and Systems

Session Chair: **Sunwoo Lee**

Session code: **B2P-F**			
No.	**Paper ID**	**Track**	**Paper Info.**
P03	7004	6	**Title:** A Wireless Neural Interface with an Implantable HEMT-LED Probe for K^+ Sensing and Optical Stimulation **Author:** **Wei Ling, Xue Shang, Xiu Zhang, Shijia Ren, Siyu Wu, Shuai Zhong, Tao Tang**
	7236	6	**Title:** An Area and Power Efficient 256-Channel Neural Signal Processor IC **Author:** **Yaqian Deng, Xun Pang, Yifan Chen, Cheng Liu, Lei Yao**
	7304	6	**Title:** A Real-Time, Energy-Efficient sEMG Pose Estimation Accelerator for Dexterous Prosthetic Control **Author:** **Danjie Chen, Kang Zhao, Xirui Guo, Hanjun Jiang**

POSTER SESSION - DAY 2

Time: **11:50-13:15**
Date: **October 22, 2025, Thursday**
Venue: **Foyer**

Session - Thermal and Optical CMOS Sensing Systems

Session Chair: **Ka-Meng Lei**

Session code: **B2P-G**			
No.	**Paper ID**	**Track**	**Paper Info.**
P04	7173	6	**Title:** Investigation of Thermal Gradients and Sensing Errors in BEOL Metal-Based Temperature Sensors **Author:** **Ruixuan Yang, Yifei Xia, Yuye Yang, Jianyu Yang, Li Geng, Dan Li**
	7327	6	**Title:** A 1.05-mW 180-nm CMOS Optical Tracking Sensor Using VCSEL Speckle Imaging and Subpixel Displacement Estimation **Author:** **Zhixun Yang, Zhenzhen Liu, Ruoxue Geng, Hanjun Jiang**

Session - Emerging Memory Devices and Architectures

Session Chair: **Can Li**

Session code: **B2P-H**			
No.	**Paper ID**	**Track**	**Paper Info.**
P05	7036	9	**Title:** Copyback-Assisted Data Migration for Hybrid 3D NAND Memory Systems **Author:** **Yang Fu, Guangxu Zhang, Guangwei Xu, Zhongguang Xu**
	7168	9	**Title:** High-Bandwidth Optical Interconnection Architecture for Distributed In-Memory Computing **Author:** **Yingge Ma, Lin Bao, Fan Zhang, Yujie Chen, Gaoqi Yang, Bowen Jiang, Yingtong Ji, Haisu Zhang, Zongwei Wang, Shanguo H...**
	7034	11	**Title:** HDME: Descriptor-Driven Merge Offloading in Hybrid-Mapped NAND Flash Systems **Author:** **Guangxu Zhang, Chenxin Zhu, Yang Fu, Xi Jin, Zhongguang Xu**
	7255	9	**Title:** Interfacial Thermal Transport in β-Ga_2O_3/NiO Heterostructures: Crystal Orientation and Temperature Dependence **Author:** **Zongyue Chai, Shuo Zhang, Wenzhang Fang**

POSTER SESSION - DAY 2

Time: **11:50-13:15**
Date: **October 22, 2025, Thursday**
Venue: **Foyer**

Session - Emerging Device and Materials

Session Chair: **Chenxi Zhu, Jun WANG**

Session code: **B2P-I**			
No.	**Paper ID**	**Track**	**Paper Info.**
P06	7181	10	**Title:** HYD-JGB Binary Additive System for Low-Loss Soft Magnetic Cobalt Coatings Toward High-Frequency Signal Transmission **Author:** **Longsheng Fang, Shimiao Wang, Tao Hang**

Session - Micro-nano Optoelectronic Chips and Integrated Devices 2

Session Chair: **Weicong Na, Baolu Guan**

Session code: **B2P-J**			
No.	**Paper ID**	**Track**	**Paper Info.**
P07	7201	15.22	**Title:** VAEM: Verifiable Architectural Exploration Methodology for Transformer Unit Accelerators via LLM-Driven HLS Agents **Author:** **Meng Liu, Zhiyang Cui**

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Zhuhai Silicon Chip Technology Ltd

ADDRESS:	**Room 1206, 12th Floor, Building 20, Xiangzhou Chuanggang Center, No. 199 Weikang Road, Xiangzhou District, Zhuhai City, Guangdong Province, China**
CONTACT PERSON:	**Lydia Yu**
MARKETING SPECIALIST:	**Marketing Operations Specialist**
TEL:	**17324706265**
EMAIL:	**lydia.yu@sichiptech.com**
WEBSITE:	**http://www.sichiptech.com**

DESCRIPTION OF THE COMPANY:

SiChip(Zhuhai Silicon Chip Technology Ltd) specializes in the development and productization of EDA tools for 2.5D/3D IC advanced packaging. It is the first company in China to deliver a complete, end-to-end EDA toolchain for 3D IC backend design. The R&D team has been working on 2.5D/3D stacked chip design methodologies since 2008, making it one of the earliest teams in the world to enter this frontier field.

The company's independently developed 3Sheng® Integration Platform(2.5D/3D IC EDA) is a full-flow platform covering the entire 2.5D/3D IC design process. It integrates five core modules: architecture design, physical design, multi-die test and fault tolerance, analysis and simulation, and multi-chiplet verification. The platform follows the STCO (System-Technology Co-Optimization) methodology. It has been proven in advanced packaging production, covering the full flow from design to manufacturing. It is now commercially deployed at several IC design companies in China, supporting the development of AI chip, GPU, CPU, silicon photonic and and high-end end-user applications.

The company has also launched Chips Z, a 3D IC EDA AI agent deeply integrated with the 3Sheng® Integration Platform. Chips Z transforms the company's deep technical expertise in advanced packaging into intelligent design capabilities.It supports collaborative system design across multiple scenarios, and can automatically connect the entire workflow while iteratively optimizing the results.

SiChip has undertaken multiple major government-backed semiconductor projects in China, accumulated nearly 100 intellectual property filings, contributed to the development of several national industry standards. The company is building a global strategy anchored in Singapore, having established partnerships with local universities and research institutes. Looking forward to working with Singapore's industry partners to drive innovation and shared growth in the global semiconductor industry.

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Marvell Asia Pte Ltd

WEBSITE: https://www.marvell.com/company/sales.html

DESCRIPTION OF THE COMPANY:

Marvell develops and delivers semiconductor solutions that move, store, process and secure the world's data. As a leader in essential data infrastructure semiconductor technology trusted by the top data center operators and OEMs, Marvell silicon powers innovation in cloud and AI, carrier infrastructure, and enterprise networking markets. With a comprehensive portfolio of compute, interconnect, network switching, security and storage products and IP, the company offers merchant, semi-custom and full-custom options to address a range of customer requirements.

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Polytec South-East Asia Pte Ltd

ADDRESS:	**Blk 4010 Ang Mo Kio Ave 10, #06-06 TechPlace 1, 569626**
CONTACT PERSON:	**Ivan Low**
MARKETING SPECIALIST:	**Marketing Strategist**
TEL:	**+65 6451 0886**
EMAIL:	**i.low@polytec.com**
WEBSITE:	**www.polytec.com**

DESCRIPTION OF THE COMPANY:

Polytec Southeast Asia provides advanced optical measurement solutions for semiconductor research, development and manufacturing across the region.
As part of the global Polytec group, founded in Germany in 1967, we support customers with high-precision, non-contact measurement technologies designed to solve complex engineering and quality challenges.
For the semiconductor industry, Polytec solutions support applications across **front-end, back-end and advanced packaging processes**, including:

- 3D surface topography and profile measurement
- Warpage, flatness and form analysis
- Step height and surface roughness measurement
- MEMS and microstructure characterization
- Dynamic vibration and frequency response measurement
- Non-contact inspection of delicate and miniaturized components

Our technologies help engineers and researchers better understand surfaces, structures and dynamic behavior—from wafers and MEMS devices to dies, packages, interconnects and electronic components.
Through our Southeast Asia team, Polytec provides **local application support, technical consultation, demonstrations and measurement solutions** to customers across the region.

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Wintech Nano-Technology Services Pte Ltd

ADDRESS:	**10 Science park Road, #03-26 The Alpha, Singapore Science Park II, Singapore 117684**
CONTACT PERSON:	**Zhang Xi**
MARKETING SPECIALIST:	**Deputy General Manager**
TEL:	**67777354**
EMAIL:	**Zhangxi@wintech-nano.com**
WEBSITE:	**www.wintech-nano.com**

DESCRIPTION OF THE COMPANY:

WINTECH NANO was founded in Singapore in 2004 and currently has multiple labs in Singapore and China. The company specialises in providing third-party semiconductor analysis services through professional and efficient one-stop Failure Analysis (FA), Material Analysis (MA), Reliability Analysis (RA), and other analysis services to customers in the semiconductor industry.

As a key technological support platform for research, development, manufacturing, and quality control in the semiconductor field, the company helps customers identify defects in product design or processes, assisting customers in improving their product yield and performance. With a wide range of testing and analytical capabilities, the company is often known as the "IC Hospital."

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KEYSIGHT — Keysight Technologies

ADDRESS: **Keysight Technologies Singapore (Sales) Pte Ltd**
1 Yishun Ave 7, Singapore 768923

CONTACT PERSON: **Stanley Mo**

MARKETING SPECIALIST: **Market Initiative Manager**

TEL: **+65 62157636**

EMAIL: **Stanley-yc_mo@keysight.com**

WEBSITE: **https://www.keysight.com/**

DESCRIPTION OF THE COMPANY:

Keysight Technologies is a global leader in electronic design, test, measurement, and simulation solutions, helping engineers and researchers accelerate innovation across semiconductor, communications, aerospace, defense, automotive, AI, quantum, and advanced electronics industries. With solutions spanning the entire product lifecycle, from research and design to validation, manufacturing, and deployment, Keysight enables customers to develop higher-performing and more reliable technologies while reducing complexity and time-to-market. Its expertise in RF and wireless systems, high-speed digital technologies, semiconductor device characterization, electronic design automation (EDA), and system-level validation empowers organizations to bring next-generation products to market faster and with greater confidence.

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Silicon Laboratories International Pte Ltd

ADDRESS: **18 Tai Seng Street, #05-01, Singapore 539775**

CONTACT PERSON: **Shantonu Bhadury**

MARKETING SPECIALIST: **Senior Design Engineering Director**

TEL: **+65 96375769**

EMAIL: **Shantonu.Bhadury@silabs.com**

WEBSITE: **https://www.silabs.com**

DESCRIPTION OF THE COMPANY:

Silicon Laboratories Inc. operates as a semiconductor company. The Company designs, develops, and markets mixed-signal integrated circuits microcontrollers, wireless connectivity devices, and sensor products. Silicon Laboratories offers solutions for automotive, retail, entertainment, and data center sectors

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Superam Academy of Semiconductor Technology

Brightecs Innovation Pte. Ltd.

ADDRESS: **11 North Buona Vista Drive, #13-07, The Metropolis Singapore 138589**

CONTACT PERSON: **Joy Tan**

MARKETING SPECIALIST: **Admin Manager**

TEL: **9233 6872**

EMAIL: **JOY.TAN@SUPERAMTECS.COM**

WEBSITE: **www.bipsuperamtecs.com**

DESCRIPTION OF THE COMPANY:

Brightecs Innovation PTE. LTD. is a newly established，technology-oriented startup. The company's core business is currently focused on silicon IP for intelligent computing mainly including a R&D center named Superam Research Institute.

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MediaTek Singapore Pte. Ltd

ADDRESS:	**1 Fusionopolis Walk, #03-01 Solaris North Tower, Singapore 138628**
CONTACT PERSON:	**Wong Sheng Jau**
MARKETING SPECIALIST:	**Senior Manager**
TEL:	**+65 93660109**
EMAIL:	**shengjau.wong@mediatek.com**
WEBSITE:	**https://www.mediatek.com**

DESCRIPTION OF THE COMPANY:

MediaTek (TWSE: 2454) is a global leader in fabless semiconductor design, providing solutions from the edge to the cloud. Powering over 2 billion connected devices every year, MediaTek's leading-edge technology keeps the world connected and enhances everyday life. At the forefront of innovation, MediaTek drives advancements in transformative technologies such as AI, 5G/6G, and Wi-Fi 7/Wi-Fi 8. Our high-performance, power-efficient products form the foundation for a smarter, more connected world, enabling devices from smartphones, smart homes and AI PCs to high-performance computing, automotive, and AI data centers. As a trusted partner to the world's leading brands, MediaTek leads the industry in creating solutions that meet the evolving needs of the global community, ensuring access to world-class technology for everyone. Our commitment to accelerating AI underscores our dedication to enriching the future of humanity. Visit http://www.mediatek.com for more information.

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GlobalFoundries

ADDRESS:	**60 Woodlands Industrial Park D Street 2, Singapore 738406**
CONTACT PERSON:	**Gn Fang Hong**
MARKETING SPECIALIST:	**Sr Director Ecosystem Enablement**
TEL:	**+66702789**
EMAIL:	**FangHong.GN@globalfoundries.com**
WEBSITE:	**www.gf.com**

DESCRIPTION OF THE COMPANY:

GlobalFoundries (GF) is a leading manufacturer of essential semiconductors, enabling AI at scale from the cloud to the physical world. We innovate to deliver differentiated, power-efficient, high-performance solutions for high-growth markets including automotive, smart mobile devices, Internet of Things, communications infrastructure and data centres. With global manufacturing operations across the U.S., Europe and Asia, GF is a trusted and holistic technology partner for customers around the world. GF Singapore is proud to be a five-time Great Place To Work certified company, a winner of multiple workforce transformation and community awards, and a Top 300 firm on the Singapore Opportunity Index. Find out more at gf.com.

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Infineon Technologies Asia Pacific Pte Ltd

ADDRESS:	**8 Kallang Sector Singapore 349282**
CONTACT PERSON:	**Tjia Jerome**
MARKETING SPECIALIST:	**VP R&D Officer**
TEL:	**6876 2090**
EMAIL:	**Jerome.Tjia@infineon**
WEBSITE:	**www.infineon.com**

DESCRIPTION OF THE COMPANY:

Semiconductors are crucial to solve the energy challenges of our time and shape the digital transformation. This is why Infineon is committed to actively driving decarbonization and digitalization. As a global semiconductor leader in power system and IoT, we enable game changing solutions for green and efficient energy, clean and safe mobility, as well as smart and secure IoT. We make life easier, safer, and greener. Together with our customers and partners. For a better tomorrow.

MEMO

IEEE ICTA 2026 Program Overview

Time / Venue	Waterfront Grand Ballroom		
	Waterfront 1	**Waterfront 2**	**Waterfront 3**
Day 1 (Wednesday, 21st October 2026)			
08:00 - 17:30	Registration, Level 2, Waterfront Foyer.		
08:30 - 08:35	Opening & Welcome Speech by Prof YEO Kiat Seng , ICTA 2026, General Chair		
08:35 - 08:40	Speech by Prof. LU Yen, ICTA 2026, TPC Chair		
08:40 - 09:20	**Keynote Speech 1:** Prof Aaron Voon-Yew THEAN ： National University of Singapore (Singapore)		
09:20 - 10:00	**Keynote Speech 2:** Prof James C. M. HWANG. ： Cornell University, Ithaca, New York (USA)		
10:00 - 10:20	**Coffee/Tea Break (Waterfront Ballroom Foyer)**		
10:20 - 11:50	**A1L-A :** High Performance RF Building Blocks	**A1L-B :** Advanced Memory for Compute, Search, and Intelligence	**A1L-C :** SS15.10: Advances in RFIC Design: Integrated Passive and Active Components for Next-Generation Systems
11:50 - 13:00	**Lunch and Poster Session (Waterfront Ballroom Foyer)**		
13:00 - 14:30	**A3L-A :** Data Converter Techniques	**A3L-B :** DC-DC Converters	**A3L-C :** SS15.11: Advanced Millimeter-Wave to Sub-THz Architecture, Circuits and Systems for Next-Generation Communication
14:35 - 15:55	**A4L-A :** SS15.21:Sensors, Sensing Circuits and Systems	**A4L-B :** Chips and Systems for Intelligent Robot and Embodied AI	**A4L-C :** SS15.6: Research Trends of RF Power Devices
16:00 - 17:15	**A5L-A :** SS15.15: AI-Era Optical Interconnects: Electronic-Photonic Co-Design and integration	**A5L-B :** SS15.13: Power IC Technology for AI Data Centers	**A5L-C :** SS15.2: Spintronics Computing and Logic
17:15 - 17:40	**Coffee/Tea Break (Waterfront Ballroom Foyer)**		
1740 - 1830	**Panel Session :** Reimagining Education in the AI Era: Bridging Academia and Industry		
1830 - 2100	**Welcome Reception**		
Day 2 (Thursday, 22nd October 2026)			
08:00 - 17:30	Registration, Level 2, Waterfront Foyer.		
08:40 - 09:20	**Keynote Speech 3:** C S CHUA ： Infineon Technologies Asia Pacific Pte. Ltd. (Singapore)		
09:20 - 10:00	**Keynote Speech 4:** Chao CHEN ： Suzhou Chuangjie Intelligent Technology Co., Ltd. (China)		
10:00 - 10:20	**Coffee/Tea Break (Waterfront Ballroom Foyer)**		
10:20 - 11:50	**B1L-A :** Modeling, Simulation & Thermal Analysis	**B1L-B** : Packaging, Reliability, and Emerging Devices	**B1L-C :** SS15.5:RF, Millimeter-Wave and Terahertz Integrated Circuits for Wireless Communication and Sensing
11:50 - 13:00	**Lunch and Poster Session (Waterfront Ballroom Foyer)**		
13:00 - 14:30	**B3L-A :** SS15.1: Breakthrough in Ultra-Broadband 5G/6G Communication Chips	**B3L-B :** AI Accelerators for DNN and Transformers	**B3L-C :** SS15.3: Communication, packaging and hybrid Integration in AI area：Theories, Algorithms, and Applications
14:35 - 15:55	**B4L-A :** SPAD Imaging and Advanced Sensor Interfaces	**B4L-B :** EH, WPT, and Gate Driver	**B4L-C :** RF Front-End and Frequency Generation
16:00 - 17:30	**B5L-A :** SS15.17: Next-Generation Wireless Technologies for Biomedical and IoT Applications	**B5L-B :** SS15.19: Compute-in-memory architectures, circuits and devices for next-generation AI systems	**B5L-C :** SS15.16: Domain-specific Hardware Design for Perception of UAVs, Humanoid Robots and Autonomous Vehicles
18:30 - 19:00	**Cocktail Reception (Waterfront Ballroom Foyer)**		
19:00 - 22:00	**Banquet Dinner (Waterfront Ballroom and Riverfront Ballroom)**		
Day 3 (Friday, 23rd October 2026)			
08:00 - 14:00	Registration, Level 2, Waterfront Foyer.		
08:30 - 10:00	**C1L-A :** In-memory Computing Devices	**C1L-B :** Design Automation and Optimization	**C1L-C :** SS15.9: Evolving RF, mm-Wave, and THz Front-Ends for Next-Generation Sensing and Communication Systems
10:00 - 10:10	**Coffee/Tea Break (Waterfront Ballroom Foyer)**		
10:10 - 11:40	**C2L-A :** Efficient Accelerators for AI and Cryptography	**C2L-B :** Domain Specific and AI Assisted Ics	**C2L-C :** High-Speed Wireline and Optical Circuits
11:40 - 12:30	**Lunch (Waterfront Ballroom Foyer)**		
12:30 - 14:00	**C4L-A :** SS15.12: Advanced CMOS RF and mmWave Frond-end Circuits	**C4L-B :** SS15.4: IC based modules, system integration and applications	**C4L-C :** SS15.8: Energy-Efficient Circuits and Systems for Intelligent Sensing and Wireless Data/Energy transfer
14:05 - 15:20	**C5L-A :** Emerging Semiconductor Devices	**C5L-B :** Analog Circuit Techniques	**C5L-C :** SS15.14: Millimeter-Wave and Terahertz Signal Generation for Next-Generation Communications and Sensing
15:25 - 16:55	**C6L-A :** SS15.18: Advanced Power Delivery for AI Computing: System Architectures, Modeling, and Converter Innovations	**C6L-B :** OpenPDK - Global FOSS Scholar Platform	**C6L-C :** SS15.20: Innovative Circuits and Systems: From Sensing to Intelligent Computing
Day 4 (Saturday, 24th October 2026)			
09:50 - 11:00 10:20 - 11:30	The Albatross File Exhibition @ Level 10 National Library Building (NLB) | Meeting Venue: **Level 1 Lobby, National Library Building, 100 Victoria Street, Singapore 188064**		